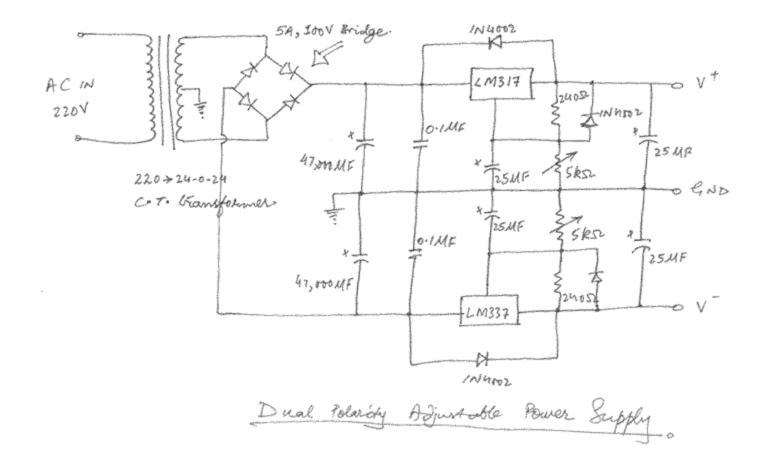
Orcad Tutorial

1. Introduction

Orcad is a suite of tools from Cadence for the design and layout of printed circuit boards (PCBs). We are currently using version 9.2 of the Orcad suite. This document will give you a crash course in designing an entire circuit board from start to finish. This will be a very small and simple circuit, but it will demonstrate the major concepts and introduce the tools behind completing a PCB design. After you have completed this tutorial, you will know all the steps needed to make PCBs using Orcad.

The circuit you will design is shown in the figure below. It is a dual polarity adjustable power supply. A center tapped transformer, some diodes, 2 IC's and few resistors and capacitors are included in the circuit.



Orcad really consists of two tools. Capture is used for design entry in schematic form. Layout is a tool for designing the physical layout of components and circuits on a PCB. During the design process, you will move back and forth between these two tools.

WARNING : Save your work frequently while working on this tutorial.

<u>NOTE</u> : It is recommended that you read this tutorial in 1024x768 display resolution.

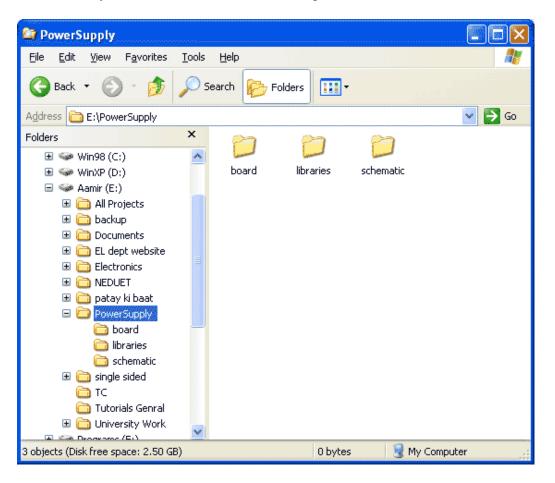
2. Before You Begin

It is helpful to be very organized when you are designing. First thing is to have a separate folder for every project. If you have a folder called Projects on your drive, don't put all your projects directly in that folder or you will create a mess that will waste your time in locating a particular file of a particular project. Instead you must have a new subfolder in it for your every project. Also Orcad will create many types of files for a single project and if you keep all of them in the same directory, it can quickly become very confusing. I like to make a directory hierarchy and put associated files into subdirectories. As you will progress working in Orcad you will realize the importance of this strategy.

So ready for some action and create a folder called **PowerSupply** on a convenient location on your drive because you are going to browse it several times during this whole tutorial. Then create inside the **PowerSupply** folder three new folders.

- schematic for your schematic files.
- libraries for symbol and footprint libraries.
- board for your board files.

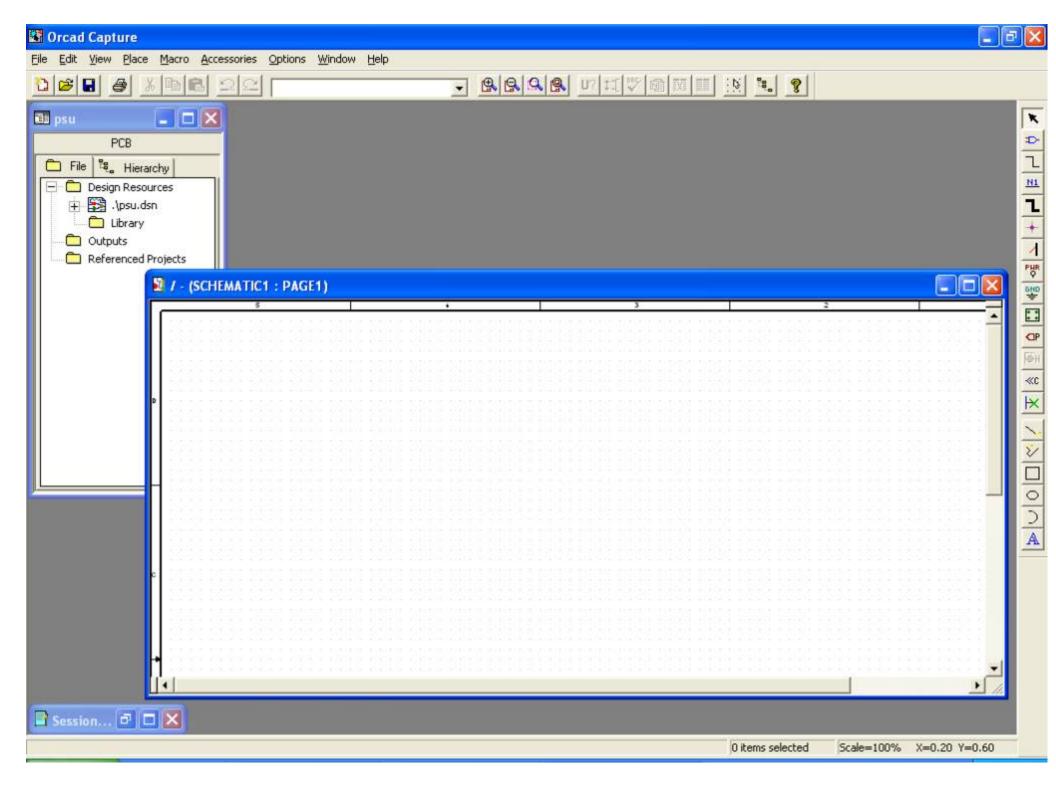
Your directory structure should look like the figure below.



3. Starting a New Schematic Project

New Project	
Name psu Create a New Project Using Image: Second Wight of the second wig	OK Cancel Help Tip for New Users The PC Board Wizard is the quickest way to get started designing a system-level schematic design
L <u>o</u> cation E:\PowerSupply\schematic	Biowse

To create a new project, first start Orcad **Capture CIS** then click **File** \rightarrow **New** \rightarrow **Project**. You will see the following dialog box. Browse to the **PowerSupply**schematic directory that you created and name the project **psu** (short for Power Supply Unit). The project name is more important than the name of your project folder. It is used as the name of all the files in your project. So give the project a meaningful and short name. Select the **PC Board Wizard** radio button and click **OK**. In the next dialog box uncheck **Enable project simulation**. Click **Next** and then remove all libraries from RHS then click Finish. You should see an empty schematic page and a project window like the following.



4. About Libraries and Parts

Orcad allows you to have libraries of part symbols for use in schematic entry. These libraries are kept in separate files that are included in the project workspace. This allows you to reuse libraries in other designs. Enormous parts are already in existing Orcad libraries. You can use these parts directly from these libraries. Open your schematic page from the Project window if it is not open. Your schematic is located in **psu.dsn** \rightarrow **SCHEMATIC1** \rightarrow **PAGE1** in the project window. Now click on the $\stackrel{\square}{\Rightarrow}$ **Place Part** tool from the right toolbar. The following dialog box appears.

Place Part		
Part:		ОК
Part List:		Cancel
		Add Library
		Remove Library
		Part <u>S</u> earch
		<u>H</u> elp
Lįbraries:	Graphic	
Design Cache	♥ <u>H</u> ormal ♥ <u>Convert</u>	
	Packaging	
	Parts per Pkg: 1	
	Pert 💽	
	Туре:	

This dialog box currently displays only the **Design Cache.** To use any of the part from Orcad built-in libraries, you need to add the library in which the part resides. Click on the **Add Library** button. Orcad Capture keeps all of its libraries in the path:

C:\Program Files\Orcad\Capture\Library

Browse to the said path and you will see many libraries. Libraries can be categorized by their name. For example, the **Gate** library contains all the digital logic gate IC's. Select the **Discrete** library and click **Open**. Now in the **Place Part** dialog box, you will see the **Discrete** library as well. Type **R** in the **Part** textbox. This will scroll down the **Parts List** to the part named **R** (i.e. the resistor). You will see the symbol of a resistor in the preview area. Then preview the capacitor by typing **C**. Now add another library named **Amplifier**. Preview its parts also. Preview as many parts as you like.

Now I will demonstrate you, how to find a part if you don't know in which library it resides. We will be searching for one of the IC's in our circuit. Click the **Part Search** button. Browse to the above-mentioned path of Orcad libraries and in the **Part Name** type *LM317* and click **Begin Search**. The two asterisks that enclose LM317 are wildcards and are necessary to include any parts in the search results that contain LM317 anywhere in their name.

art Search		
Part <u>N</u> ame:		
LM317		OK
Libraries:		Cancel
LM317/CYL/Regulator.olb LM317/DD/Regulator.olb	^	Begin <u>S</u> earch
LM317/DPAK/Regulator.olb LM317/S0/Regulator.olb		Help
LM317/SOT/Regulator.olb LM317/TO/Regulator.olb		
LM317/T0220/Regulator.olb LM317/T0263/Regulator.olb		
Library Path:		

Scroll down to the part named LM317/TO220 (because we are using the TO-220 package for the LM317 IC) and click OK. The Regulator library is now added to Place Part dialog box. Preview the required part LM317/TO220.

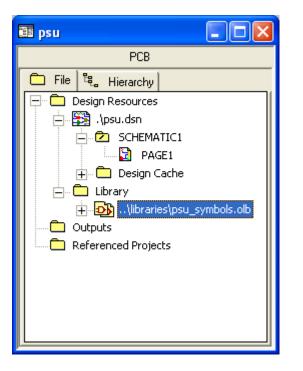
Place Part		
<u>P</u> art:		_ ОК
LM317/T0220		
Part List:		Cancel
LM309/T039		Add Library
LM313/TO LM317/CYL LM317/DD		Remove Library
LM317/DPAK LM317/S0 LM317/S0T LM317/T0 LM317/T0220		Part <u>S</u> earch ▼ Help
Libraries:		
AMPLIFIER Design Cache DISCRETE REGULATOR	Graphic © <u>N</u> ormal © <u>C</u> onvert	
INCOULATION	Packaging Parts per Pkg: 1 Part Type: Homogeneous	ADJ «Value»

Previewing different parts was only a demonstration. Select all the libraries and click the button **Remove Library.** You will note that all the libraries can be removed except the **Design Cache.**

5. Creating a Schematic Parts Library

Orcad allows you to create your own libraries of part symbols. You can create symbols for those parts, which you are unable to find in Orcad libraries, or you want to draw a part symbol according to your own standard and convenience. We will now create symbols for some of the parts in our design and use the rest from the Orcad built-in libraries.

For this we have to add a new library to our design. To do this, highlight the **psu.dsn** in the project window and click **File→New→Library**. Right-click the **library1.olb** file in the project window and select **Save As...** Name the file **psu_symbols** and place it in the **libraries** directory that you created earlier. Your project window will now look like the figure below. You are now ready to add parts to your library



6. Creating Schematic Symbols

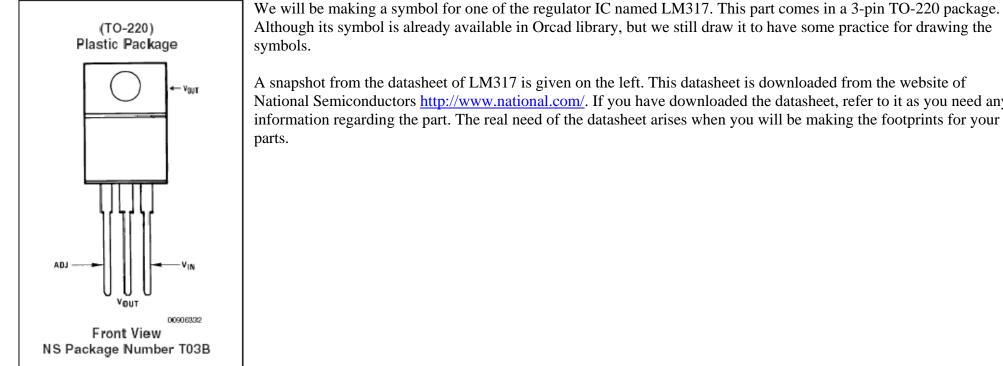
To add a new part to your library, right-click the library file and select **New Part**. This will bring up a dialog box for **New Part Properties**. Make the entries in the dialog box so that it looks like the following.

New Par	rt Properties		
<u>N</u> ame:	LM317		ОК
Part <u>R</u> efe	rence Prefix:	2	Cancel
PCB Foot	print:		Part <u>A</u> liases
Multiple	e Convert View •Part Package oer Pkg: 1		Attach Implementation
Pacl	kage Type Homogeneous Heterogeneous ERSUPPLY\LIBRAR	Part Numbering Alphabetic Numeric IES\SYMBOLS.OLB	Pin Number Visible

Click **OK** to bring up the workspace for part creation. It should look like the picture below. Tools for working with the part are located on the toolbar on the right-hand side of the screen.

👪 Orcad Capti																		E	
<u>E</u> ile <u>E</u> dit ⊻iew	1.	1.4	1 1						124.1	1 sectors				a 1999a I					
	3 Ⅰ Ⅰ		20	GND			<u> </u>	9 9 9		17 年11 🏹	國國		10 H.	?					
Di psu	PC8 Hierarchy		- 01	X															Г Ц Ц
E Design	n Resources \psu.dsn	s	ymbols.olt																티치페 기상ロ이이족
		317	V																
Outpr				17	2	2	U	?	10	17	2	7	20	2	-	122		T I I	
	- 2																		
	- 25																		
							<	Val	lue	>									
0											_	_	_	_	_		2		
Session	о, [Ц [Х	J										_	0 items :	selected	Scale	e=459%	X=0.70	0 Y=-0.10	0

WARNING: Before you begin drawing your part or start making entry in your schematics, make sure that "Snap to grid" feature is activated. If it is activated then the "Snap to grid" button on the top toolbar will look like this 🔝. Otherwise it will turn red 📕 to warn you that this feature is deactivated. If it is deactivated, it will cause serious difficulties in your schematic entries.

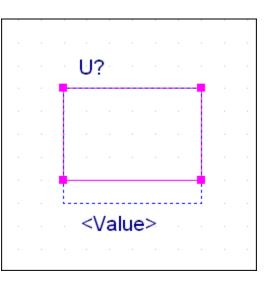


A snapshot from the datasheet of LM317 is given on the left. This datasheet is downloaded from the website of

National Semiconductors http://www.national.com/. If you have downloaded the datasheet, refer to it as you need any information regarding the part. The real need of the datasheet arises when you will be making the footprints for your

First we draw the outline of the IC, which is a rectangle. So select the **rectangle** tool and draw a rectangle. After you have drawn it, you should have something like the figure on right.

Now we will draw the pins of the IC. Click on the **Figure Pin** tool to place pins on the part. You will see a dialog. Make it looks like the figure below.

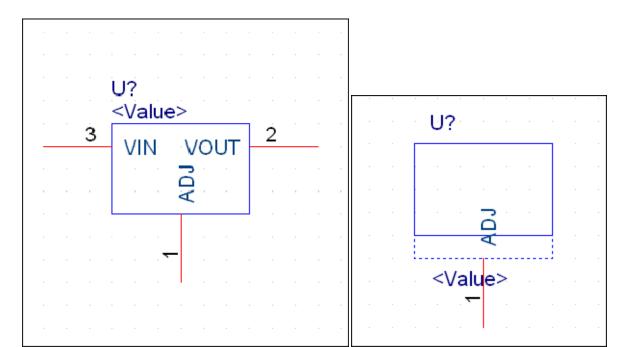


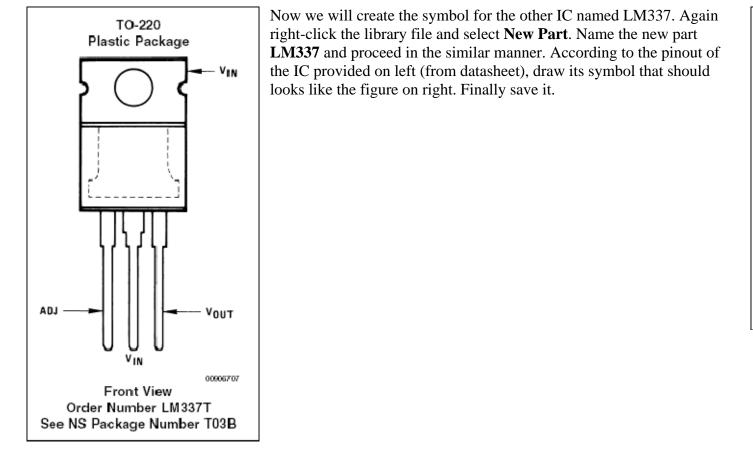
Shape:	OK
Line	Cancel
Passive 💌	User Properties
M Pin Visible	<u>H</u> elp
	Line _ Iype: Passive _

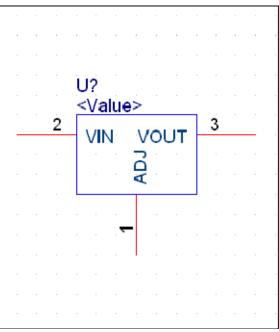
Click **OK** and place the pin below the bottom side of the dotted outline like the following figure on left

Refer to the part datasheet for the correct pin numbers and pin names for the TO-220 package. Create the rest of the two pins in the similar manner. Adjust the size of dotted outline and the rectangle you just created if necessary such that they both coincide with each other. To do this, click on the outline of the dotted box or the rectangle and then drag one of the corners to expand or contract it. Also position the **part reference** and the **value** to a suitable place. You should end up with something like the figure on right.

Save your part and close the window. Your part will now be visible in your library.







Congratulations! You have successfully created two symbols in your new library. Now we will not draw any more symbols. The Orcad libraries are here to make your life easy. It is usually OK to use parts directly from Orcad libraries

7. Schematic Entry

You are now ready to start placing the electrical components for your design. The circuit that we will be drawing is shown in the beginning of this tutorial in

the hand drawn form. We will need all the parts that are included in that circuit diagram. Open up the schematic page and click the Place Part tool on the toolbar on the right side of the screen. Here you will have to add those libraries, which contain your desired parts. As a novice designer, you might experience difficulties in finding a particular part because there are so many libraries and thousands of parts in each of them. But you can always do away with this difficulty if you carefully read the library name. The **Part Search** feature will certainly be very helpful in these circumstances.

WARNING: Again make sure that "Snap to grid" feature is activated.

For this design, add two Orcad built-in libraries named **Discrete** and **Connector**. Now you have the **Place Part** dialog box having three libraries and **Design Cache** like the figure below.

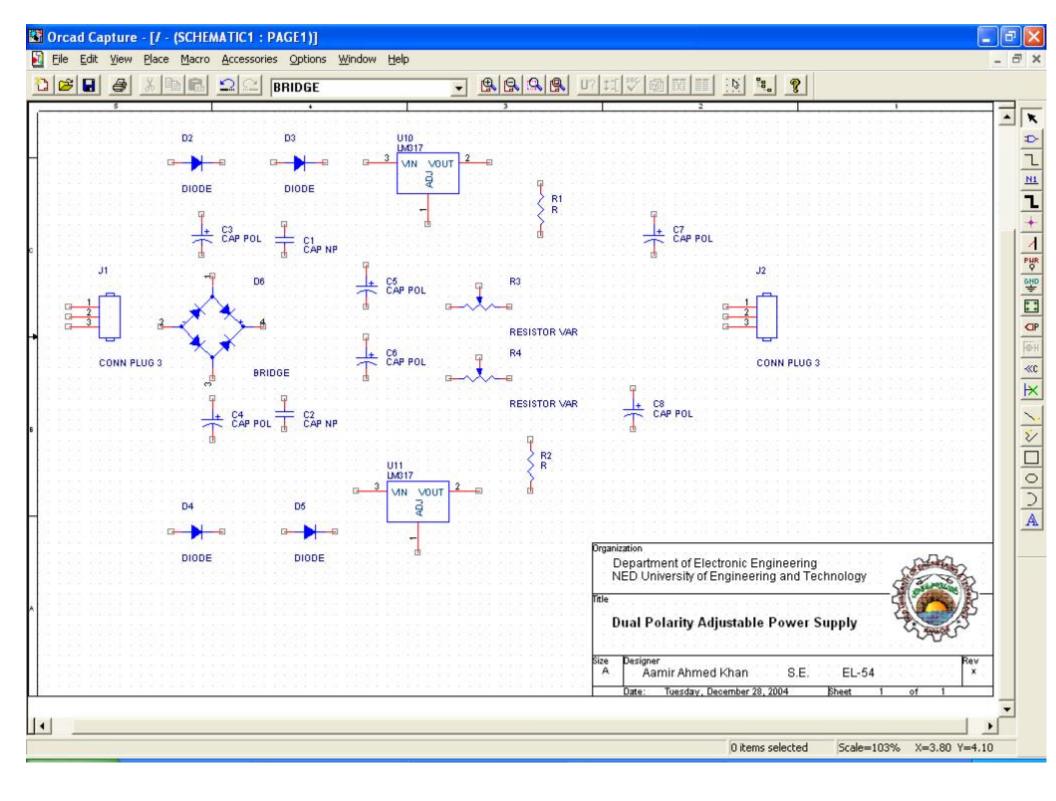
Place Part		
Part:		- OK
Part List:		Cancel
12 HEADER	<u></u>	Add Library
4 HEADER 8 HEADER B2S		<u>R</u> emove Library
B25 BNC BNC-2 CIRDIN_13-P CIRDIN_13-R CIRDIN_13-P	~	Part <u>S</u> earch <u>H</u> elp
Libraries: CONNECTOR Design Cache DISCRETE PSU_SYMBOLS	Graphic Graphic Convert Packaging Parts per Pkg: 1 Part: Type: Homogeneous	

Select the **Connector** library and type **CONN PLUG 3** in the **Part** textbox to select this part and then click **OK**. Place the part on the left side of your schematic page. Take your cursor to the right of schematic page and click once more. The **CONN PLUG 3** part is placed two times. Press the **<Esc>** key or

right-click then select **End Mode** to exit the part placement mode of the cursor. Then again click the Place Part tool and from psu_symbols library, select LM317 and place it. Similarly place LM337. Also from Discrete library, add the following parts indicated times:

•	R		2
٠	CAP NP		2
٠	CAP POL		6
٠	RESISTOR VAR	2	
٠	BRIDGE		1
٠	DIODE	1	

After placing all the indicated parts your page should look like this.



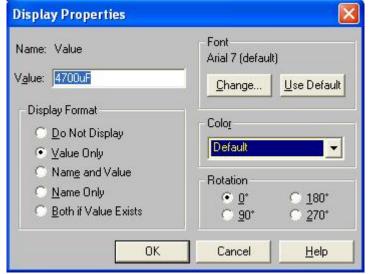
You will probably be wondering why we have not placed the transformer in our schematic. The reason is simple. A transformer is a heavy and bulky part. It is rarely mounted on a PCB. If it were mounted on the PCB, its heavy weight would easily snap or crack the PCB. Our schematic should contain only those parts that are supposed to appear on the PCB. The part **J1** will be joined to the three leads coming from the secondary of the center-tapped transformer and the transformer itself will be mounted somewhere else on the chassis.

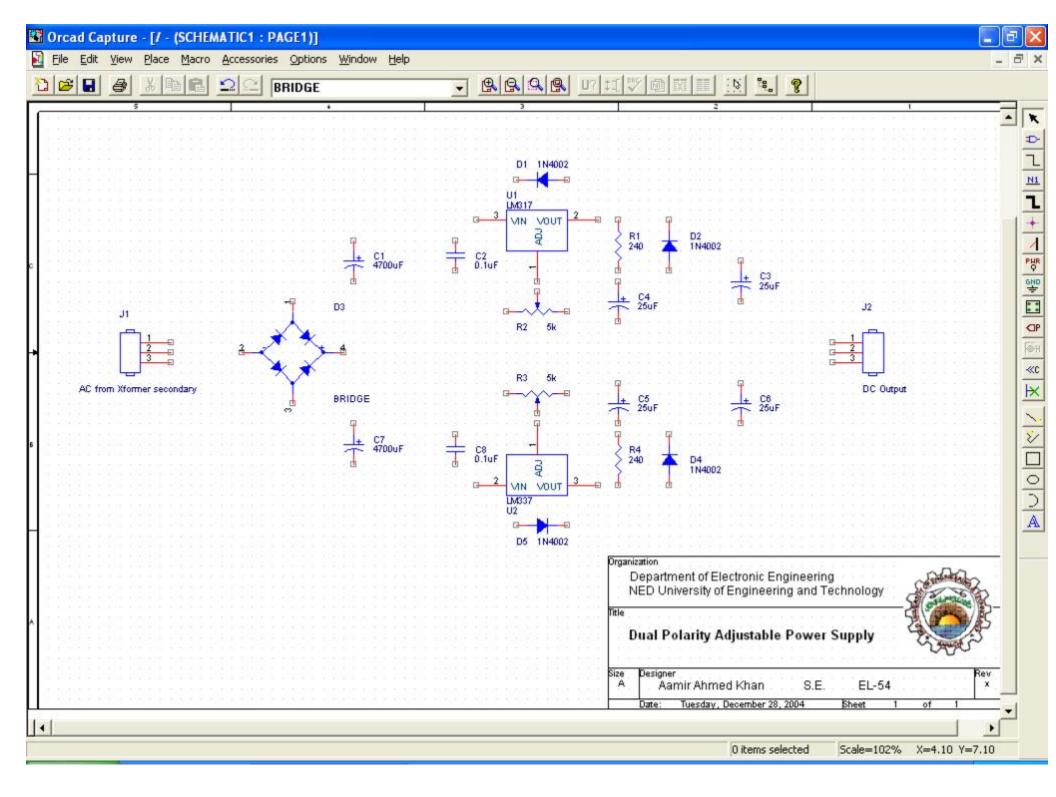
A small hint for moving around in Orcad: use 'I' and 'O' to zoom in and out, respectively. 'C' will center the design at your cursor. 'R' will rotate a part. 'H' and 'V' will mirror the part horizontally and vertically respectively. You can do these actions while in the middle of another action (e.g. while placing a part or while wiring the parts). You will also notice that each part has two texts associated with it. One is **Part Reference** and the other is the **Value**. You can change them by double-clicking the text. See figure on right. In this manner you can give all your capacitors, resistors, etc. the appropriate values. At this stage, don't change the **part reference** of any part (See the NOTE below). Place these texts in a position that look nice. Also place and orient the components as indicated in the figure below, because in the next step, we are going to make connections between the parts. If the parts are placed in an organized manner, it will be much more easier to interconnect these parts. (Hint: Vertically mirror **LM337** and the **variable resistor** close to it while horizontally mirror **J1**)

<u>NOTE</u>: The term **Part Reference** is more than often referred to as the **<u>Reference Designator</u>**. You should keep this term in mind. It is extensively used in the further discussion. You can

understand **Reference Designator** as a label to refer a part in your design. It consists of two parts – a prefix and a number e.g. C5. The prefixes like R, C, SW, Q, U etc. identifies the type of the part. There are no absolute rules for assigning the prefixes to parts but conventions still exist. You can assign prefix Q to a resistor and U for a diode but it will violate the convention that Q and U are reserved for transistors and IC's respectively. The number that follows the prefix is used to differentiate between different parts of the same type having same prefix.

When you are done, the first page of your schematics should look something like the figure below. Don't panic if the reference designators in your schematic do not match the following figure. It will be fixed up later. But don't attempt to change them.





Now we need to draw nets to make electrical connections between components. To do this, click the **Place Wire** tool or press **Shift+W** or from **Place** menu click **Wire**. Click once at the pin of a part and then release the mouse button. Move the cursor, clicking once for each 90⁰ bend in the wire, to the desired pin of the other part and click there. The two pins will be connected successfully. Connect the components as shown in the figure of completed schematic given below.

You may also want to add ground connections to some of the parts. Orcad has a built-in

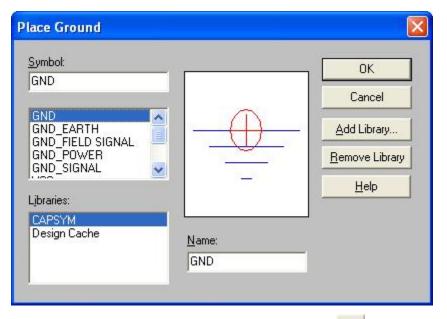
library for power and ground symbols. Click the Place Ground tool. This will open up the Place Ground dialog box. You will need only CAPSYM library for all of your power and ground symbols. So remove all libraries here and then add CAPSYM. Select the GND symbol here and click OK. Place the GND symbol two times in the schematic and connect them as shown in completed schematic.

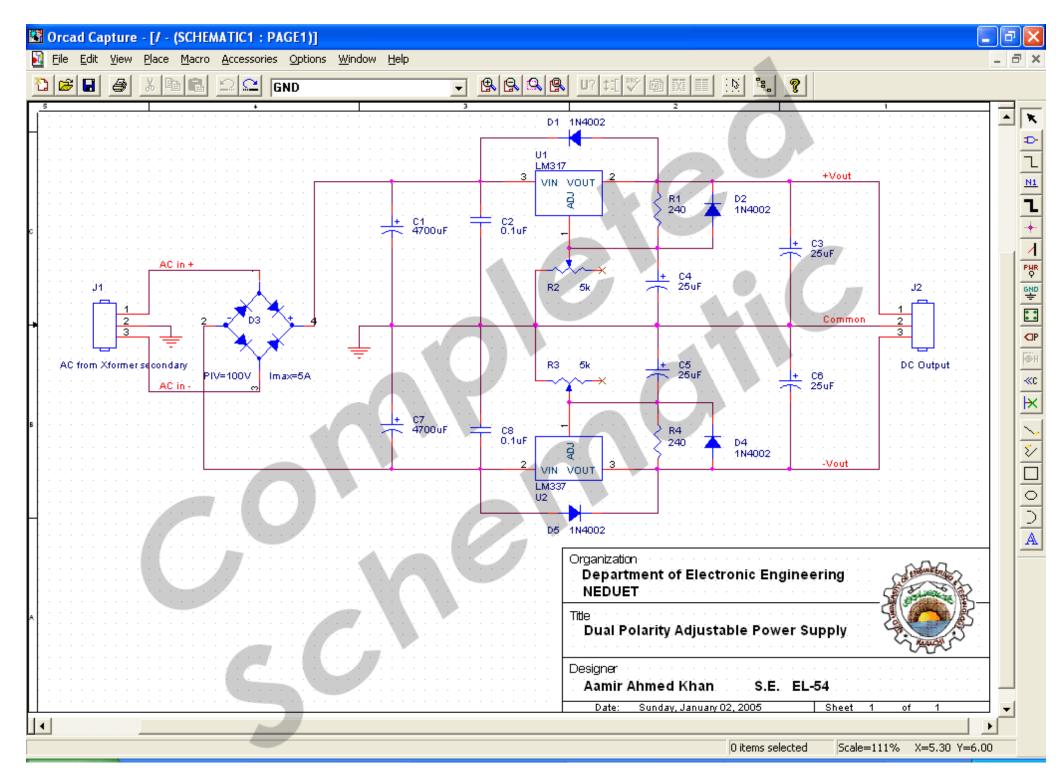
After you have drawn all the nets according to the completed schematic figure below, there will remain two pins of the variable resistors unconnected. In Capture you must add a NC marker (No Connection) to all the unconnected pins, or they will generate errors.

To do this click on **Place no connect** tool and place the marker on both the pins.

It is a good design practice to name the important nets in your schematics. This is extremely useful and can help tremendously in the layout process. I encourage you to name any important nets such as supply, ground, inputs, outputs, clocks, address and data

bus lines, and other specific signals you are interested in. To name a net, first highlight the net (i.e. wire) you want to name and then click the **Place Net Alias** tool, you will be given a dialog box to enter the name of the net. You can position the text above the net anywhere you like. Remember, if you give the two different nets a same name, the two nets will be electrically shorted together. Now name the nets that are named in the completed schematic.





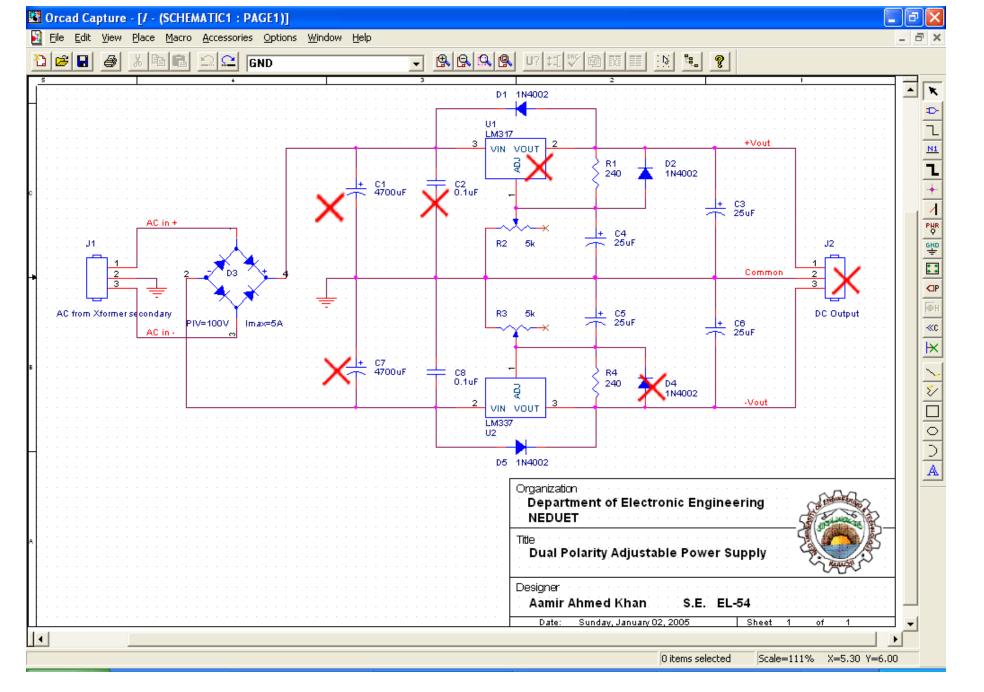
Congratulations! The schematic entry is now complete, means that you have completed one of the three phases of your project. Save your work.

8. Preparing for Layout

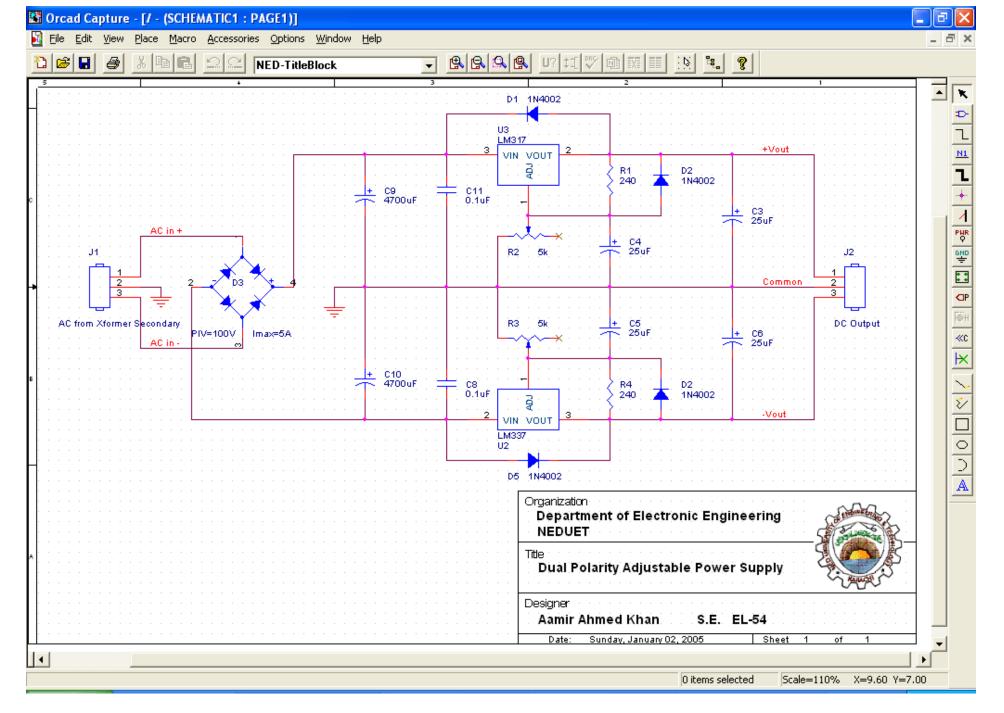
The transference phase (transferring the design from Capture to Layout) is the second phase of your project and is very crucial. Annotating your design is the first step of this phase

8.1 Annotation

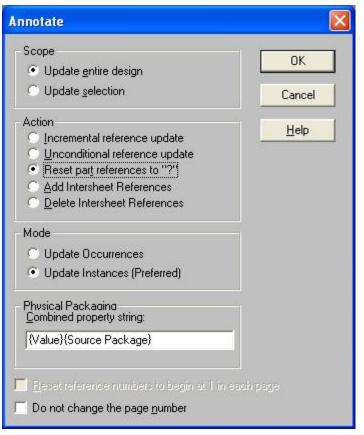
To introduce the concept of annotation, delete the six parts from your schematic that are marked with a red cross in the following figure.



Then place the deleted parts again from the **Place Part** tool except the diode. Copy and paste **D2.** Don't undo. It won't help you understand the concept. Change the values of newly placed parts (not the reference designators) to the previous ones according to the completed schematic figure. Place the parts at their previous locations and wire them again. Now you will have your schematic in the following condition.



You should realize that your schematic is spoiled as far as reference designators are concerned. Note that the series of capacitors begin from C3 instead of C1 and also within the series, C7 is missing. After J1, there is J3 instead of J2. An even worse problem exists in case of diodes: D2 is present twice. These errors hamper the transference of your design to the Layout. Remember! These sort of nasty errors would always arise, whenever you copy-paste or delete the parts in your schematic.



Annotation is a process to rectify these errors. Save the schematic and close it. In the File view of the project explorer, highlight the top-level design file (the one with the **dsn** extension) and then select **Tools**->**Annotate**. You will see the **Annotate** dialog box. In a design that is being annotated for the first time, it is best to first reset all the reference designators. To do this, click the radio button that says **Reset Part References to "?"** Make all other options like the figure on right and then click **OK**. Click **OK** for what you will be asked. Every part in your design will now have a question mark in its reference designator instead of a number. But ? indicates that it will be replaced by a number in the next step of annotation.

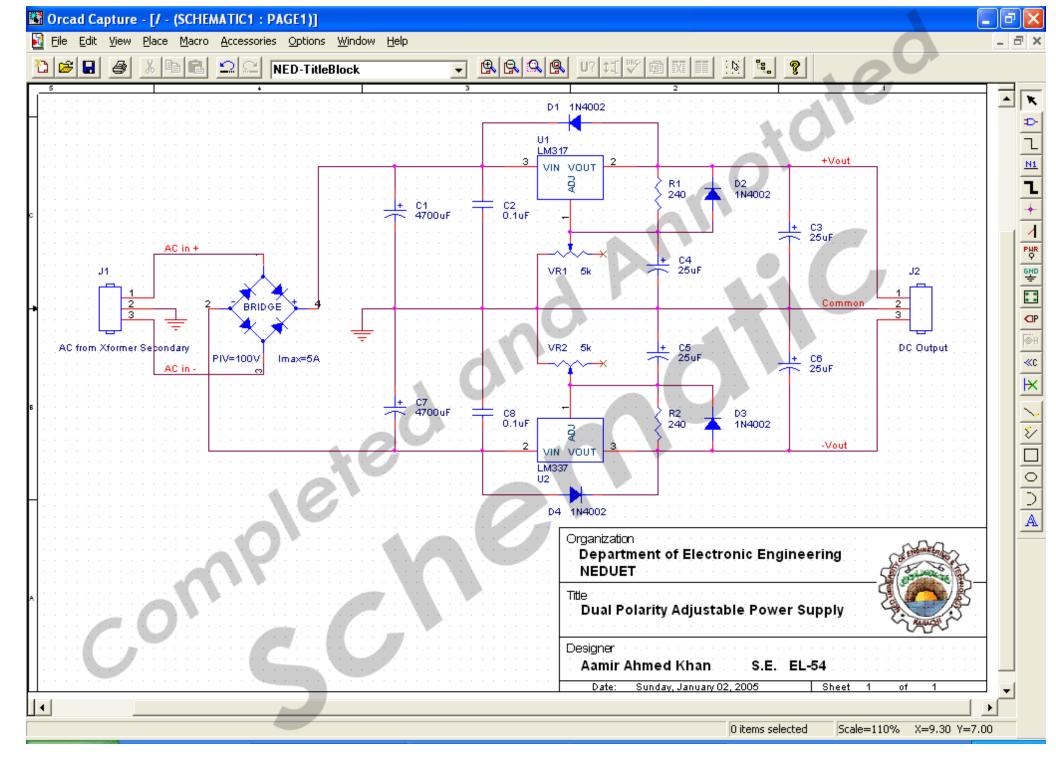
Now, this is the right time to edit any of the reference designators if you like. For example, you might want to change the reference designator of the bridge so that there is no number in its reference designator being the only bridge in the design e.g. from **D**? to **BRIDGE**. Perhaps you are also thinking about changing the reference designator of variable resistors from **R**? to **VR**? Go ahead and change the above mentioned reference designators by double clicking and changing them.

Now return to the process of annotation. Reopen the annotate dialog box and check the box that says **Incremental Reference Update** and click **OK**. This will go through your entire design and number each

part starting with 1 for each part type. If you now look in the hierarchy view of the project explorer, you will see that you have a nicely ordered list of parts. See figure on left.

After the annotation is complete, your schematic will look like this.

aa psu	
	PCB
🗀 File 🖁	🐛 Hierarchy
	HEMATIC1
Ð	BRIDGE (PIV=100V IMAX=5A)
	C1 (4700UF)
	C2 (0.1UF)
	C3 (25UF)
	C4 (25UF)
	C5 (25UF)
	C6 (25UF)
	C7 (4700UF)
	C8 (0.1UF)
	D1 (1N4002)
	D2 (1N4002)
	D3 (1N4002)
	D4 (1N4002)
	J1 (AC FROM XFORMER SECONDARY)
	J2 (DC OUTPUT)
	R1 (240)
	R2 (240)
	U1 (LM317)
	U2 (LM337)
	VR1 (5K)
D	VR2 (5K)



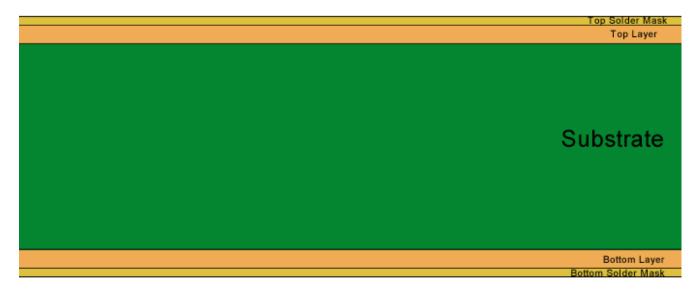
8.2 Creating Footprint Libraries

A footprint is the representation of the physical area that a component occupies on a PCB. Your next step will be to design footprints for all the parts in your circuit. Like Capture, Layout has also several built-in libraries of footprints. But unlike Capture libraries, I suggest you not to use the Layout libraries as a novice designer. The reason is that the names of Layout libraries and the footprints contained within them are very cumbersome and confusing to understand. There is also no option of searching these libraries. It is better that you yourself design footprints of your components. This will ensure you that the footprints you are using are correct. Once you will get enough knowledge and experience about the packaging of electronic components, so that you will be able to locate the desired footprint in these libraries then you can, of course, use them.

Warning: I cannot overemphasize this point. It is absolutely crucial that your footprints are correct. Double-check them, triple-check them. It is sometimes possible to live with an error in a schematic symbol, but a footprint error can often sink your entire design.

Before making a footprint it is necessary to understand a little bit about how PCBs are constructed.

PCBs consist of a number of electrical and non-electrical layers. 2 to 4 electrical layers are fairly common for simple circuit boards. 8 to 20 layers can often be seen in many industry applications. In our lab, we have the facility to fabricate two layers boards i.e. double sided PCB's. The diagram below shows the layer stackup for a 2-layer board like the one you are making now. The layers are defined below



Double sided PCB

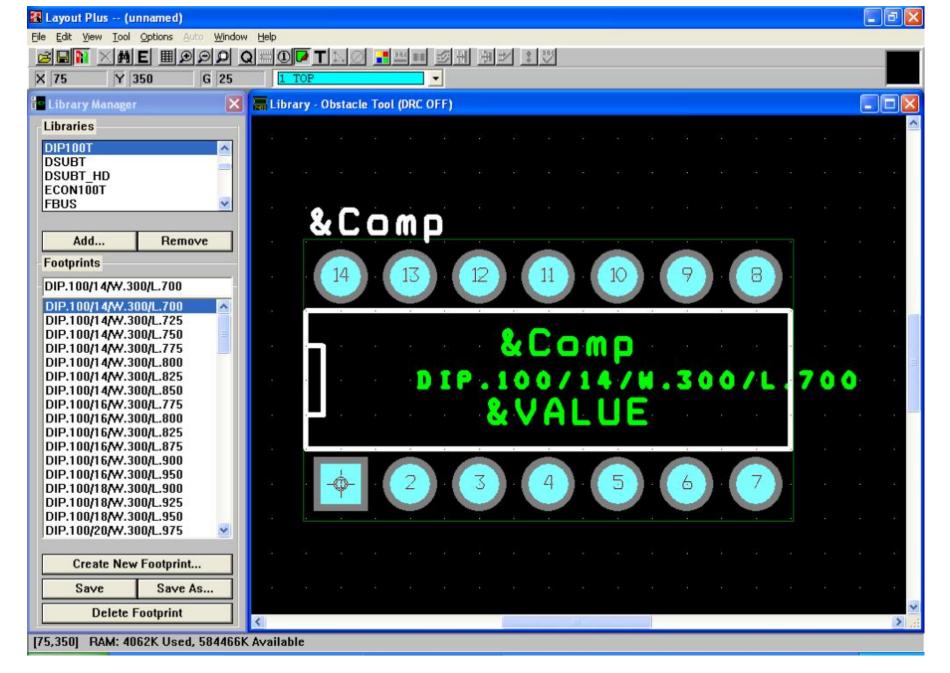
- Top and Bottom Layers are sheets of copper and used for routing nets between parts.
- Solder Mask is a coating on the top and bottom of the PCB to prevent solder from flowing freely on the board. It also protects copper tracks from oxidation and provides insulation. This is what gives most circuit boards their green or brown color.
- Substrate is made up of bakelite, fiberglass or epoxy resin dielectric material. It separates the two layers and also gives stiffness to the board.
- Drill Layer This layer defines finished drill sizes and drill locations for parts that have pins that go through the board.

• Silkscreen is used for documentation of a PCB. Reference designators and other useful text can be printed on the top or bottom of a PCB using a process similar to that used for silkscreen t-shirts.

Start Orcad Layout. Layout has a separate tool for working with footprint libraries. To start this tool, select **Tools**->Library Manager. In the new window that opens, you will notice that there are already several libraries available for use. These are the built-in libraries. For designing a footprint, you can use either of the two approaches:

- 1. Use the mechanical information contained in the component datasheet.
- 2. Manually measure the size of the component, distance between its pins and their dia. This is only possible if you have the component at your disposal at this step.

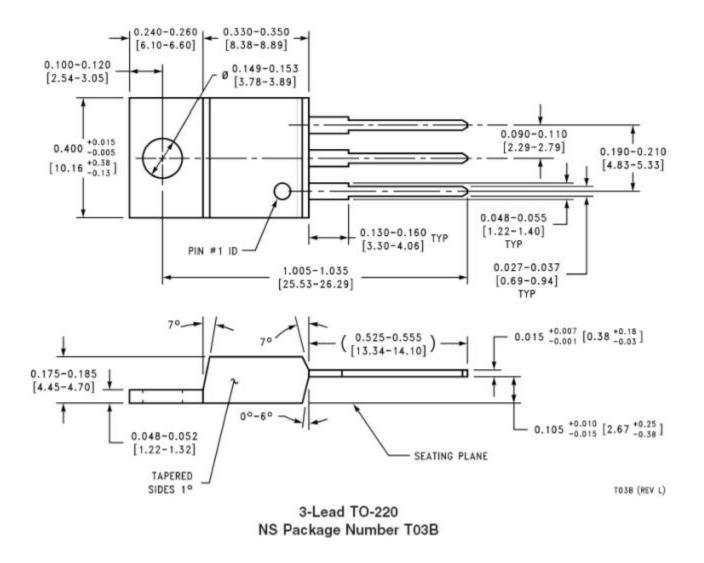
Footprints are composed of one or more padstacks. These padstacks define how a pin on a part looks on each of the electrical and non-electrical layers. Each of your footprints will need at least one padstack defined. Let's take a look at a padstack definition for an existing part. In the **Library Manager**, select the library **DIP100T** and highlight the first part **DIP.100/14/W.300/L.700**. You will see the part footprint in the **Library Manager**.



Layout uses a series of spreadsheets to store information about your design. Padstacks are stored in the padstack spreadsheet. To access this spreadsheet, click the **III** View Spreadsheet icon and choose Padstacks. This footprint is composed of two padstacks, one for pin 1, which is square, and another padstack for the other pins. When you open the spreadsheet, you will first see a padstack called **T1**. Padstacks **T1** to **T7** are default padstacks and can be modified for your own use. The padstacks we want to look at are at the bottom of the list; scroll down until you see **DIP100T.llb_pad1** or **DIP100T.llb_pad2**. These are the two padstacks for this footprint. You will notice that there are numbers on some of the layers that define how the padstack looks physically on that particular layer. We will come back to this in a minute.

Close the padstack spreadsheet and open up the footprints spreadsheet. The name is confusing; it should really be called something like the pins spreadsheet because this spreadsheet defines the locations of the pins and also which padstack they use. You will see each pin for the part in this spreadsheet, its x and y locations, and the padstack used for each pin. Notice that pin 1 uses the square padstack, while the others use the round one.

Now let's create a new footprint from scratch for your design. We will make the footprint for **LM317** IC. The same footprint will be used for **LM337** IC. The mechanical diagram of the TO-220 package of the IC from its datasheet gives us all the information we need to know.



In the Library Manager, click Create New Footprint. This will bring up the following dialog box. Name the footprint TO-220 REGULATOR IC, and keep English for the Units. Click OK to create the part. You will now see a new part with just one pin and lots of text in the Library Manager.

If you like to switch to Metric units from English, then select **Options→System Settings** to bring up the following dialog. Change the systems settings as shown. But I recommend that you work in English system of units because most PCB fabrication measurements are still done in inches or mils.

Always remember the following conversions.

1 inch = 2.54 cm
1 inch = 1000 mils
1 mm = 39.37 mils
1 mm = 40 mils (used for quick estimates)

Click **Cancel** because you will be working in English units.

The IC has 3 pins, but we only need to define one padstack since the pins are all the same physically (not electrically). Open the **padstacks** spreadsheet. We will edit the padstack **T1**, which is already being used by pin1. First, let's start from scratch and fill in information for only the layers that we care about. In the spreadsheet, double-click the padstack name **T1**. This brings up the **Edit Padstack** dialog for all layers in the padstack.

First, change the name of the padstack to something like **PSU_HOLE**. Next, select the **Undefined** radio button. This will reset the padstack definitions on

System Settings		×				
Display Units	Grids					
○ <u>M</u> ils (m) ○ <u>I</u> nches (in)	Visible grid [X,Y]:	1				
○ <u>M</u> icrons (u) ⊙ <u>M</u> illimeters (mm)	De <u>t</u> ail grid [X,Y]:	.1				
C Centimeters (cm)	Place grid [X,Y]:	.1				
Display Resolution:	<u>R</u> outing grid:	.1				
0.0254	<u>V</u> ia grid:	0				
Rotation Increment: 90 Snap: 01'						
<u>W</u> orkspace Settings <u>O</u> K <u>H</u> elp <u>C</u> ancel						

every layer. Click OK to continue. In the spreadsheet you should now see a padstack called REGULATOR_PIN with no layers defined.

We will now set each layer individually. You can also select multiple layers at a time by holding down the **CTRL** key when you click the layer name. First, let's define the size of the drill used for this part. The datasheet tells us that the pin dia can vary from 0.027 to 0.037 in. So we should use a drill of dia greater than 37 mils. Let us use a drill of 40 mils. Select the layers **DRLDWG** and **DRILL**. When you have multiple layers selected, you will need to right-click and choose **Properties** or press **CTRL**+**E** to bring up the **Edit Padstack** dialog. Choose the **Round** radio button and give the width and height a value of 40. Click **OK** when done. The changes you made should now be reflected in the spreadsheet.

Now we will define the amount of metal on the routing layers beyond the size of the drill. This is called the annular ring. Each board shop will have requirements on the minimum annular ring size based on the drill diameter. In most cases 20 mils is a safe bet. Select the **TOP**, **BOTTOM** layers and bring up the **Edit Padstack** dialog. Make the pads round and put the value of 60 (40+20 mils) in the height and width fields.

The last thing we need to define is the solder mask. This is usually defined as slightly larger (about 5 mils) that then annular rings on the top and bottom layers. Select **SMTOP** and **SMBOT** and make them round pads with height and width of 65 (60+5 mils).

You have finished defining your padstack for this part. Your Padstacks spreadsheet should now look this.

🦉 Padstacks					
					^
Padstack or	Pad	Pad	Pad	X	
Layer Name	Shape	Width	Height	Offset	
PSU_HOLE					
ТОР	Round	60	60	0	
воттом	Round	60	60	0	
PLANE	Undefined	0	0	0	
INNER	Undefined	0	0	0	
SMTOP	Round	65	65	0	
SMBOT	Round	65	65	0	
SPTOP	Undefined	0	0	0	
SPBOT	Undefined	0	0	0	
SSTOP	Undefined	0	0	0	
SSBOT	Undefined	0	0	0	
ASYTOP	Undefined	0	0	0	
ASYBOT	Undefined	0	0	0	
DRLDWG	Round	40	40	0	
DRILL	Round	40	40	0	
COMMENT LAYER	Undefined	0	0	0	
SPARE2	Undefined	1 0	0	0	
SPARE3	Undefined	Ő	Ő	0	
T2					
ТОР	Square	62	62	0	
<]					> .

You can close the spreadsheet and you will see that pin 1 should now look a little different based on the changes you just made. You probably noticed that you don't need to define all of the layers. As a guide, here are the layers that you need to define for thru-hole technology (THT) and surface mount technology (SMT) parts.

- THT components: TOP, BOTTOM, SMTOP, SMBOT, DRLDWG, DRILL
- SMT components: TOP, SMTOP, SPTOP

As far as padstacks are concerned, surface mount parts are a lot easier to work with. But we will rarely work with SMT parts because they require special equipments for soldering.

Now click **Save**. Since you are saving this footprint for the first time, you will be asked to select the library to keep the footprint in. You have not yet created a footprint library, so you will need to click the **Create New Library** button. Browse to your **libraries** directory and name the library **PSU_FOOTPRINTS**.

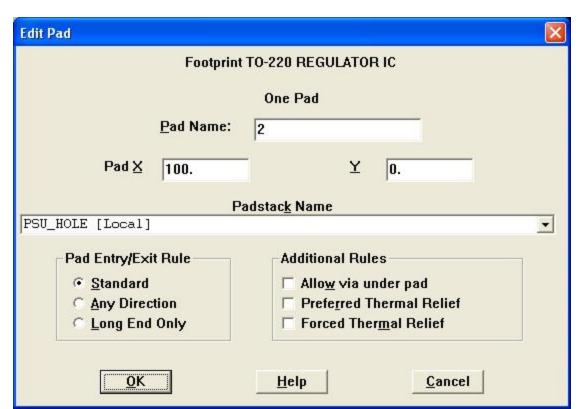
Let's now clean up a few things before adding the rest of the pins. You will see a lot of text on your screen. Most of it is on the layer **ASSYTOP**, which we will not use. This text is safe to delete. Open the text spreadsheet and you will see five text items. Select all the text on the **ASSYTOP** layer and delete them. This will clean up your footprint a bit. You can leave the reference designator text on the **SSTOP** layer. We will need it.

Before creating all the pins for a part, please make note of a few things. The name of the pad is very crucial. It **MUST MATCH** the **number** property of the corresponding pin in the schematic symbol. To know what are the pin numbers, open your schematic in **Capture** and double click U1 i.e. LM317. Click the **Pins** tab and select **Orcad-Capture** in the drop-down box. Now look at the **Number** property. It should look like the figure below. Hence the pin numbers for your IC are 1, 2 and 3. Most of the time, the pins are numbered as 1,2,3,4... but this is not always the case.

		Name	Number	Net Name	Туре
1 🕞	SCHEMATIC1 : PAGE1 : U1 : VOUT	VOUT	2	+Vout	Passiv
2 🛃	SCHEMATIC1 : PAGE1 : U1 : VIN	VIN	3	N14986	Passiv
з н	SCHEMATIC1 : PAGE1 : U1 : ADJ	ADJ	1	N038212	Passiv
_ •					

Refer to the datasheet again. The spacing between adjacent pins is given to be 90 - 110 mils. We will use the mean spacing i.e. 100 mils. We can add pins to the footprint in a number of ways, but the easiest way to do this is to use the footprints spreadsheet. Open the spreadsheet and you will see just pin 1 with an (x,y) location of (0,0). Always place pin 1 at (0,0). To create a new pin, just highlight pin 1 in the spreadsheet and type CTRL+C. This will open up the following Add Pad dialog.

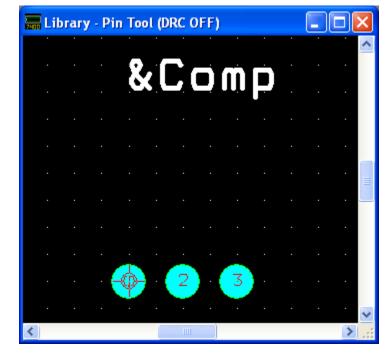
Type 2 in the **Pad name** because the next pin number in schematic symbol is 2. Type 100 as the x-coordinate to place the next pad 100 mils apart from origin i.e. pad 1. Choose the **PSU_HOLE** padstack for the pin. In most cases, you will leave the other settings as they are by default. Add the third pad in the similar manner.



The spreadsheet should now look like this.

Footprints						
Footprint Name or	Insertion	Padstack	Exit	Pad	Pad	Via
Pad Name	Origin	Name	Rule	X Loc	Y Loc	Under
Footprint TO-220 REGULATOR IC	0,0					
Pad 1		PSU_HOLE	Std	0	0	No
Pad 2		PSU_HOLE	Std	100	0	No
Pad 3		PSU_HOLE	Std	200	0	No

When you close the footprint spreadsheet, your footprint should look like this.

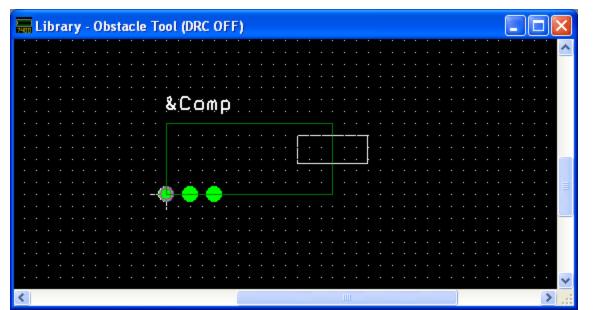


You are not quite done with the footprint even though all the pins are placed. There are just a few things left to do. First, we need to define a place outline. A place outline is a mechanical boundary that Layout uses to keep parts from hitting each other once assembled. If the IC were mounted standalone on the PCB, its outline would be easy to drawn - simply enclose all the pads with the smallest possible rectangle. But it will be mounted with a heatsink so its outline will be somewhat bigger. Mount the heatsink on IC and measure the size of the complete assembly with a Vernier Calipers or an ordinary scale. If you measure in mm, convert it to mils. The heatsink, which I am using is 18 mm (720 mils) long and has a width of 8 mm (320 mils) when mounted on IC. Currently the **detail grid** in the **system settings** dialog (press **CTRL+G** to open this dialog and check it) is set to 25 mils. This won't allow you to draw a 720x320 mils rectangle. Round off the dimensions to 700x300.

Click the **Obstacle Tool** in the toolbar to switch to the obstacle tool and then right-click in the workspace. Select **New** from the context menu. Right-click again and select **Properties**. The following dialog box appears.

Edit Obstacle			
	Obstacle <u>N</u> ame	1	
	0 <u>b</u> sta	acle Type	
	Place ou	and the second se	•
<u>G</u> roup	Heigh <u>t</u>	<u>W</u> idth	10.
	Ob	stacle <u>L</u> ayer	
	Glob	al Layer	J
- Copper Pour Ru	es		
Cl <u>e</u> arance		Zo	rder
Note: U	lse Pin Tool co	mmand 'Toggl	e Copper Pour Seed'
		pper pour see	dpoints
☐ Isolate all tra	cks r	<u>Seed only fro</u>	om designated objec
	lot <u>F</u> ill Beyond ch <u>Pattern.</u> ,	Obstacle Edg	e <u>P</u> in Attachment
<u>O</u> K		<u>H</u> elp	<u>C</u> ancel

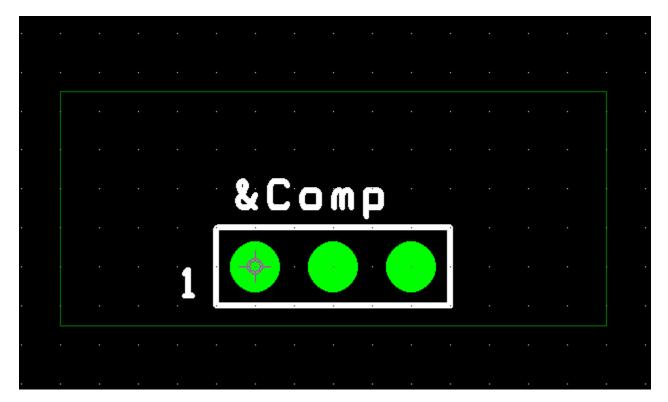
Select **Place Outline** as the **Obstacle Type**. The **Height** in this case is arbitrary. The layer is very important. This part is a thruhole part, so in this case we want to make sure that THT and SMT parts on the bottom side of the board will not interfere with this part. By choosing **Global Layer**, the place outline will extend through every layer of the board. If this were a surface mount part, we could put the place outline on the top layer only. Click **OK** when you are done making changes. Now you need to draw the outline. You can use the same shortcut keys here that you used in Capture to zoom and center the design ('I', 'O', and 'C'). Your objective is to draw a 700x300 rectangle. Start from the origin, watch out the coordinates in the status bar and left-click to place each corner. When you have drawn at least 3 corners, you can press 'F' to have Orcad finish the outline for you. Now you need



to place the outline at the correct location. For this, make a selection box at any of the sides of the obstacle to select it. See the figure on right. Now click at the corner of the obstacle, which is at the origin and drag it to the location (-250,-75).

There is just one last thing you need to do to make your footprint complete. It is often nice to have an outline of the part on the silkscreen layer too. This is not necessary, but it is a nice touch and makes things a bit easier during assembly of your board. Right click in the workspace and from the context menu, select **New**. Right-click again and select **properties**. Change the type to **Detail**, change the layer to **SSTOP** and change the width to 8. Draw the rectangle in the same way, you drew previous one but of a smaller size as shown below. Also select the **Text** tool and select the text. Press **CTRL**+**E** to set **Line width**=8 and **Text height**=50. Move the text to a suitable location as shown below. It is often nice to indicate the pin numbers of IC. While the **text** tool still activated, right-click in the workspace and select **New...** from the menu. Type **1** in **Text String** and select the **Free** radio button. Change the Line Width and Text Height to 8 and 50 respectively. Select the **SSTOP** layer. Click **OK** and place the text near pin 1 of the IC.

When you are all done, the footprint should look like this.



Congratulations! You have created your first footprint. Save it.

I have provided the rest of the footprints used in this design in another library named **ALL_FOOTPRINTS** in the **lib** folder of this tutorial. Add this library by clicking **Add** button. Browse to the **lib** folder and select the file named **ALL_FOOTPRINTS.LLB** Open this library and you will see many footprints in it. You must copy these footprints in your own library **PSU_FOOTPRINTS.** Click the ¹/₄ **W RESISTOR** footprint and click the **Save As...**

📴 Library Manager					
Libraries					
PSU_FOOTPRIN BCON100T BCON156T BGA CLCC	BCON156T BGA				
Add	Remove				
Footprints					
1/4 W RESISTOR 3 PINS PORT BOARD MOUNTING HOLE BRIDGE CERAMIC_CAP DO-41 DIODE LARGE_CAP POTENTIOMETER SMALL_CAP TO-220 REGULATOR IC					
Create New					
Save	Save As				
Delete F	Delete Footprint				

button. Select your library from the drop-down box and click **OK**. The footprint of the resistor will be copied in your library.

Save Footprint As		
Name of footprint		
1/4 W RESISTOR		
Name of Jibrary		
E:\POWERSUPPLY\LIB	RARIES\PSU_FOOTPRINTS.LLB	<u> ■</u> rowse
	Create New Library	
	Help	Cancel

Similarly copy all the footprints from ALL_FOOTPRINTS to PSU_FOOTPRINTS. When you are done the PSU_FOOTPRINTS library should contain 10 footprints and look like the figure on right.

Now remove the ALL_FOOTPRINTS library from the Libraries list.

8.3 Assigning Footprints to Parts

You will now switch back briefly to working in Capture. Open the schematic if it is not already open. You have defined a set of footprints to be used in your design, but now you must assign those footprints to each of the parts in your design. Each part in your schematics has a property called **PCB Footprint** and this must match one of the footprints in your footprint library. Double-clicking any part in schematics will open **Property Editor**. This will show you all the properties for that part. Double click **U1** in the schematic. This is the part whose footprint you just drew. Filter the properties by choosing **Orcad-Layout** in the drop-down list and make sure that you are on the **Parts** tab. You should be able to see the **PCB Footprint** property now and assign it a value of **TO-220 REGULATOR IC**, the name of the footprint you just drew.

Property Editor								
New Column Apply Display Delete Property Filter by: Orcad-Layout						Help		
	Value	Reference	Primitive	Name	Power Pins Visible	PCB Footprint	COMPFIXED	COMPC -
1 SCHEMATIC1 : PAGE1 : U1	LM317	U1	DEFAULT	122116	Γ	TO-220 REGULATOR IC	111111	11/1/2
								_
								_
Parts & Schematic Nets	A Pins	A Title Block	ks 🔏 Global	IS A PI	•			•

It is possible to assign footprints to parts in a quicker way. Close the property editor and press **CTRL+A** while on the schematic page. This will highlight every part on the page. Press **CTRL-E** to bring up the **Property Editor**. Again make sure you are on the **Parts** tab and properties are filtered by **Orcad-Layout**. Now you can see the properties for every part you have highlighted. Right click the **Value** column header and select **Sort Ascending**. Assign footprints to all the parts as shown below.

Property Editor							
New Column Apply Display	Delete Property Filter by:	Orcad-Layout			-	Help	
	Value	Reference	Primitive	Name	Power Pins Visible	PCB Footprint	COMPFIXED CO
1 SCHEMATIC1 : PAGE1 : C8	0.1uF	C8	DEFAULT	103667		CERAMIC_CAP	
2 SCHEMATIC1 : PAGE1 : C2	0.1uF	C2	DEFAULT	122094		CERAMIC_CAP	
3 E SCHEMATIC1 : PAGE1 : D4	1N4002	D4	DEFAULT	104203		DO-41 DIODE	
4 SCHEMATIC1 : PAGE1 : D2	1N4002	D2	DEFAULT	104137		DO-41 DIODE	
5 SCHEMATIC1 : PAGE1 : D3	1N4002	D3	DEFAULT	122619		DO-41 DIODE	
6 SCHEMATIC1 : PAGE1 : D1	1N4002	D1	DEFAULT	104181		DO-41 DIODE	
7 SCHEMATIC1 : PAGE1 : R2	240	R2	DEFAULT	103623		1/4 W RESISTOR	
8 E SCHEMATIC1 : PAGE1 : R1	240	R1	DEFAULT	103601		1/4 W RESISTOR	
9 E SCHEMATIC1 : PAGE1 : C4	25uF	C4	DEFAULT	103733		SMALL_CAP	
10 SCHEMATIC1 : PAGE1 : C6	25uF	C6	DEFAULT	103755		SMALL_CAP	
11 SCHEMATIC1 : PAGE1 : C3	25uF	C3	DEFAULT	103777		SMALL_CAP	
12 E SCHEMATIC1 : PAGE1 : C5	25uF	C5	DEFAULT	103799		SMALL_CAP	
13 E SCHEMATIC1 : PAGE1 : C1	4700uF	C1	DEFAULT	122050		LARGE_CAP	
14 SCHEMATIC1 : PAGE1 : C7	4700uF	C7	DEFAULT	122072		LARGE_CAP	
15 E SCHEMATIC1 : PAGE1 : VR2	5k	VR2	DEFAULT	103847		POTENTIOMETER	
16 E SCHEMATIC1 : PAGE1 : VR1	5k	VR1	DEFAULT	103821		POTENTIOMETER	
17 E SCHEMATIC1 : PAGE1 : J1	AC from Xformer Secondary	J1	DEFAULT	103469		3 PINS PORT	
18 🛨 SCHEMATIC1 : PAGE1 : J2	DC Output	J2	DEFAULT	122142		3 PINS PORT	
19 🛨 SCHEMATIC1 : PAGE1 : U1	LM317	U1	DEFAULT	122116		TO-220 REGULATOR IC	
20 E SCHEMATIC1 : PAGE1 : U2	LM337	U2	DEFAULT	105651		TO-220 REGULATOR IC	
21 SCHEMATIC1 : PAGE1 : BRIDGE	PIV=100V Imax=5A	BRIDGE	DEFAULT	109800		BRIDGE	
▼ Parts & Schematic Nets & Pins & Title Blocks & Globals & Ports & Alias							

You will notice that there is no option of specifying the name of the footprint library. So what will happen when there are two footprints in different libraries having a same name? Layout looks for the footprint named in the **PCB Footprint** property in the listed libraries from top to bottom. To move a library in the upper region of list, remove it and then add it again. This will place that library on the top of the list. It is a good design practice to make a different library for each project and then add it at the top of the list. Make new footprints or copy footprints from other libraries in that library. This will make sure that the footprints will be taken from only that library.

8.4 Creating the Netlist

To export your design to Layout, you must first create a netlist. A netlist is a file that has all the parts, footprints and nets for your design in a format that can be read by the layout program. To start netlist generation, highlight your **dsn** file and select **Tools**→**Create Netlist**... to bring up the **Create Netlist** dialog

box. Click on the **Layout** tab in the dialog box. Make the dialog box looks like the figure below and click **OK** to generate the netlist. When finished you should have a file called **PSU.MNL** in your **schematic** directory. Your design is finally ready for import into layout.

Create Netlist	
EDIF 2 0 0 PSpice SPICE VHDL Verilog	Layout NF Other
PCB Footprint Combined property string: {PCB Footprint}	
Options <u>B</u> un ECO to Layout User Properties are in inches User Properties are in <u>m</u> illimeters	
Netlist <u>F</u> ile:	
E:\POWERSUPPLY\SCHEMATIC\PSU.MNL	Browse
	OK Cancel Help
	OK Cancel Help

8.5 Creating a Board Template File

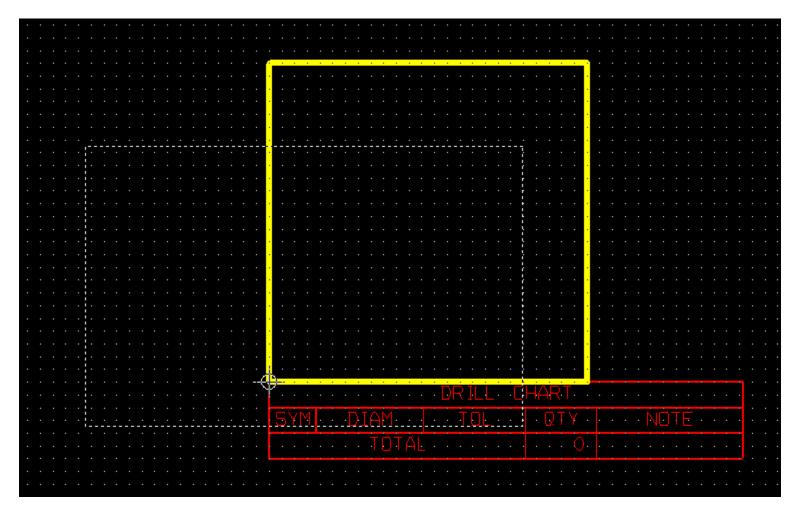
You are almost ready to export your schematic design to Layout. Before doing this, we must create a board template file because you will be asked for it when you will be exporting your design to **Layout**. This file defines some default properties for the board that will be used throughout layout. To create a template, start Layout and select **File** New. When you see the dialog, press **Cancel**. You should now see a blank workspace. You can use the same shortcut keys that you used in Capture to zoom and center the design ('I', 'O', and 'C').

ORILL CHART SYM DIAM TOL QTY NOTE TOTAL 0					
SYM DIAM TOL DIY NOTE					
SYM DIAM TOL DIY NOTE					
SYM DIAM TOL DTY NOTE					
	—		DRILL C	HART	
TOTAL	SYM	DIAM	TOL	QTY	NOTE
		TOTAL		0	

Change the system settings (**CTRL**+**G**) like the figure below.

System Settings		
Display Units Mils (m) Inches (in) Microns (u) Millimeters (mm) Centimeters (cm) Display Resolution:	Grids Visible grid [X,Y]: Detail grid [X,Y]: <u>P</u> lace grid [X,Y]: <u>R</u> outing grid:	100 25 25 25 25
Rotation	⊻ia grid: Snap: 0 1	25
, <u>₩</u> or	kspace Settings	ancel

The first thing we need to do is draw a board outline to define the perimeter of the board. For this PCB, we will make the board 2½ x 2½ inches i.e. 2500x2500 mils. The board outline is an obstacle like the ones you placed in the footprint editor. To create the board outline, select the **Obstacle Tool**, right-click and choose **New...** and then right-click again and select **Properties...** Name the obstacle **BOARD_OUTLINE**, its type should be **Board Outline**, its **Width** should be 50 (mils) and it should be placed on the **Global Layer**. Place the first corner of the board at 0,0 and then draw from there. When finished, your board outline should look like this.



Next, you will edit the layer stackup. Layout has spreadsheets just like the **Library Manager** does. Click the **View Spreadsheet** icon and select **Layers**. This spreadsheet defines all the layers that your board uses and their respective functions in the design. You are making a 2-layer board, so we will turn off some of the pre-defined layers because we will not use them. While pressing the **CTRL** key, select these layers:

GND, POWER, INNER1 – INNER12, SPTOP, SPBOT, SSBOT, ASYTOP, ASYBOT, FABDWG, NOTES.

Press **CTRL**+**E** to bring up the **Edit Layer** dialog. Select the **Unused Routing** radio button and click **OK**. Here we turned off the *SPTOP*, *SPBOT* layers because we are not using SMT components in our design. Also we will not mount parts on the bottom side of the PCB, so we turned off the *SSBOT* layer. If your design requires these layers, you should not declare them unused.

Next, you will define a default via size. Vias are used to connect tracks between layers and to make connections to solid ground or power planes. Click the **View Spreadsheet** icon and select **Padstacks**. This will open the padstacks spreadsheet and shows every padstack that is used in your design. Since there are no parts in the design right now, there are not that many padstacks, but this will change after we import from Capture.

You will edit the **VIA1** padstack that is first on the list. This will become the default via for your design. Editing padstacks here is identical to how you edited padstacks when creating a footprint. Let's start with a clean padstack. Click the name **VIA1** to highlight the entire padstack. Right-click and select **Properties** to show the **Edit Padstack** dialog. Select the radio button labeled **Undefined** and also check the box labeled **Flood Planes/Pours**. Click **OK** when done. This will reset the definitions for all layers of **VIA1**. Now you will set the finished drill size. Highlight the **DRILL** and **DRLDWG** layers and open the **Edit Padstack** dialog. Select a pad shape of **Round** and give it a width and height of 50 (mils). We are defining somewhat large vias because this PCB is of a power supply and it will contain high current carrying copper tracks. Similarly select **TOP** and **BOTTOM** layers and press **CTRL+E**. Select **Round** with a width and height of 75. Finally, highlight the **SMTOP** and **SMBOT** layers and make these round with a diameter of 80. After you are done defining this via, your spreadsheet should look like this.

\overline Padstacks

	×

						1
Padstack or	Pad	Pad	Pad	×	Y	
Layer Name	Shape	Width	Height	Offset	Offset	
VIA1]
ТОР	Round	52	52	0	0	
BOTTOM	Round	52	52	0	0	
GND	Undefined	0	0	0	0	
POWER	Undefined	0	0	0	0	
INNER1	Undefined	0	0	0	0	
INNER2	Undefined	0	0	0	0	1
INNER3	Undefined	0	0	0	0	1
INNER4	Undefined	0	0	0	0	1
INNER5	Undefined	0	0	0	0	1
INNER6	Undefined	0	0	0	0	1
INNER7	Undefined	0	0	0	0	1
INNER8	Undefined	0	0	0	0	1
INNER9	Undefined	0	0	0	0	1
INNER10	Undefined	0	0	0	0	1
INNER11	Undefined	0	0	0	0	1
INNER12	Undefined	0	0	0	0	1
SMTOP	Round	57	57	0	0	1
SMBOT	Round	57	57	0	0	1
SPTOP	Undefined	0	0	0	0	1
SPBOT	Undefined	0	0	0	0	1
SSTOP	Undefined	0	0	0	0	1
SSBOT	Undefined	0	0	0	0	1
ASYTOP	Undefined	0	0	0	0	1
ASYBOT	Undefined	0	0	0	0	1
DRLDWG	Round	32	32	0	0	1
DRILL	Round	32	32	0	0	1
FABDWG	Undefined	0	0	0	0	1
NOTES	Undefined	0	0	0	0	

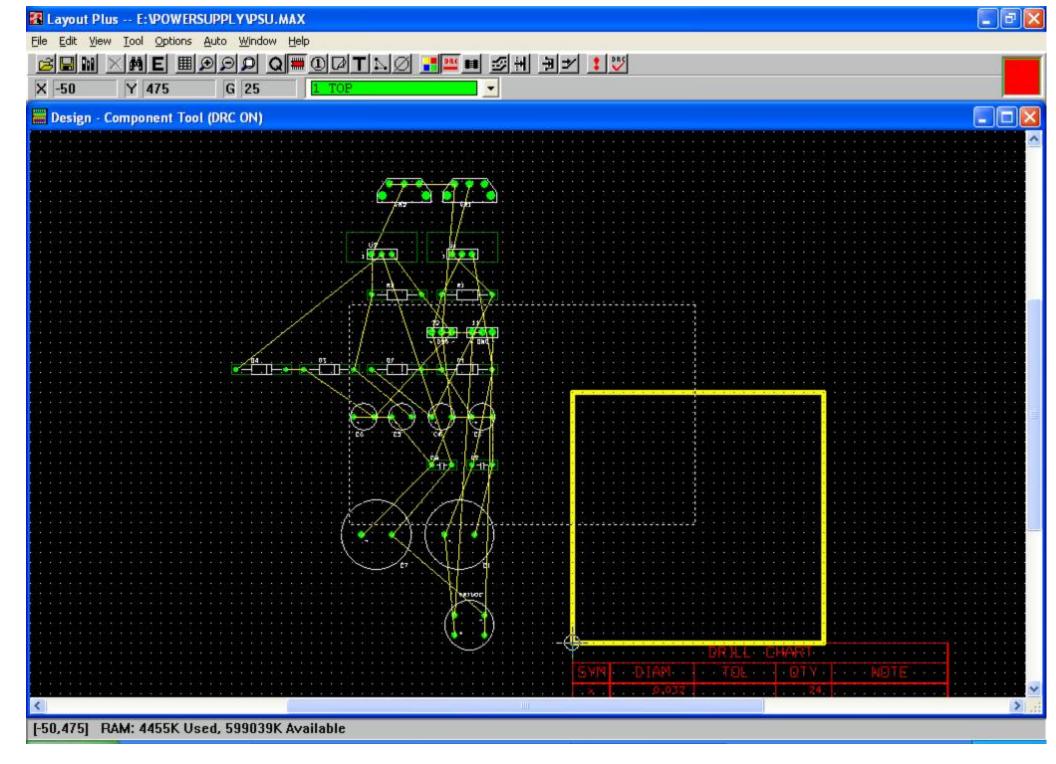
The final thing we need to do to our template is to set a few global spacing constraints. These spacing values will be used when you have Layout automatically check for design errors. Each board shop will have its own requirements on the minimum value of these constraints. Select Options->Global Spacing... to bring up the Route Spacing spreadsheet. Click on Layer Name to highlight every cell, and then right-click and select Properties to bring up the Edit Spacing dialog. Put a value of 15 in every field. Click OK and close the Route Spacing spreadsheet. Then open the Nets spreadsheet and double click the net name DEFAULT. Put a value of 15, 40 and 60 in the Min Width, Conn Width and Max Width boxes respectively. Since the PCB manufacturing facility in our department has a requirement of 15 mils on all these spacing and also on the minimum track width, that's why we used a value of 15 mils.

Save your template in your libraries folder. Name it PSU_BOARD_TEMPLATE and select the type as Template(*.tpl;*.tch). Open the Library Manager and once again make sure that PSU_FOOTPRINTS is on the top of libraries list.

9. Starting Layout

9.1 Creating a New Board

Now we have everything that we need to import our design into Layout so we can start moving on to the third phase of our project. Start Orcad Layout or Layout Plus but not Layout Engineer's Edition and select File \rightarrow New. You will first be prompted for the template file you created. It should be located in your libraries directory. Second, you will be asked for your netlist. This should be located in your schematic directory. Third, you will be asked to give your board file a name. Name this file psu and place it in the **board** directory. If all the footprint names in your design match those in your library, then you should get no errors and you will see a screen in layout like the one below.



If you got one or more errors, then it probably means that you have a misspelled footprint name in the **PCB Footprint** property in your schematic. Sometimes, you can also accidentally assign a footprint that doesn't have the same number of pins as your schematic symbol. If your import is unable to complete, then you will have to find and fix the problem and start the process again. One useful tool for finding an error is the **lis** file. When Layout performed the import, it generated a file called **psu.lis** in your board directory. Open this file in a text editor like Notepad to see what it says. This file will tell you everything that occurred during the import: what footprints, components and nets were added or deleted. If an error occurred, you will see it here, probably towards the end of the file.

9.2 Getting Around & Placing Parts

All of your parts from schematics should be line up on the left side of the board. Learn a few things about the Layout environment before you start placing these parts. First turn off **DRC** (Design Rule Check) by clicking the button to vanish the dotted rectangle. We will use it later when routing, but not now. Again you can use the same shortcut keys that you used in Capture to zoom in, out and center the design ('I', 'O', and 'C') and **SHIFT+Home** to zoom all.

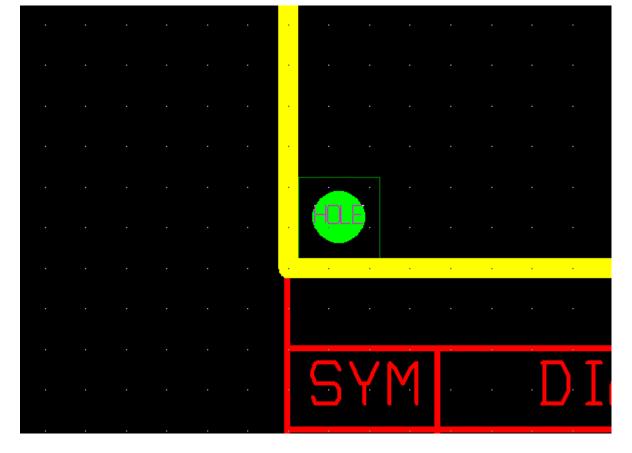
You will also notice that the workspace often gets too messy while working in Layout, so you will need to refresh the screen very often. Use the **Layout Refresh All** button or press **Home** key. Also on the toolbar, there is a drop-down box of layers. You can select any layer and turn it visible or invisible. To toggle a layer visible/ invisible, select the layer and hit the – (minus) key on your keyboard. You will also notice that there are a bunch of lines connecting your parts. These are connections that are still unrouted, and this is usually referred to as the **Ratsnest**. When placing parts, it is sometimes useful to turn this off. So click the **View Spreadsheet** icon and select **Nets**. Remember when you used this spreadsheet before? It had just one net called **DEFAULT**. Now, every net in your design should appear in this spreadsheet. This spreadsheet can be a useful way to see if you have misnamed nets in your schematics. Highlight every net by clicking the cell labeled **Net Name**. Right-click and choose **Properties**. Uncheck the **Routing Enabled** box and click **OK**. The ratsnest should have disappeared.

You are now ready to place parts on your design. To get into parts placement mode, make sure that the **Component Tool** is selected. In addition to placing the components that are in your schematics, you can also place non-electrical components right in Layout. You will do that now to place some mounting holes on your board. While using the **Component Tool**, right-click and select **New** to bring up the **Add Component** dialog box.

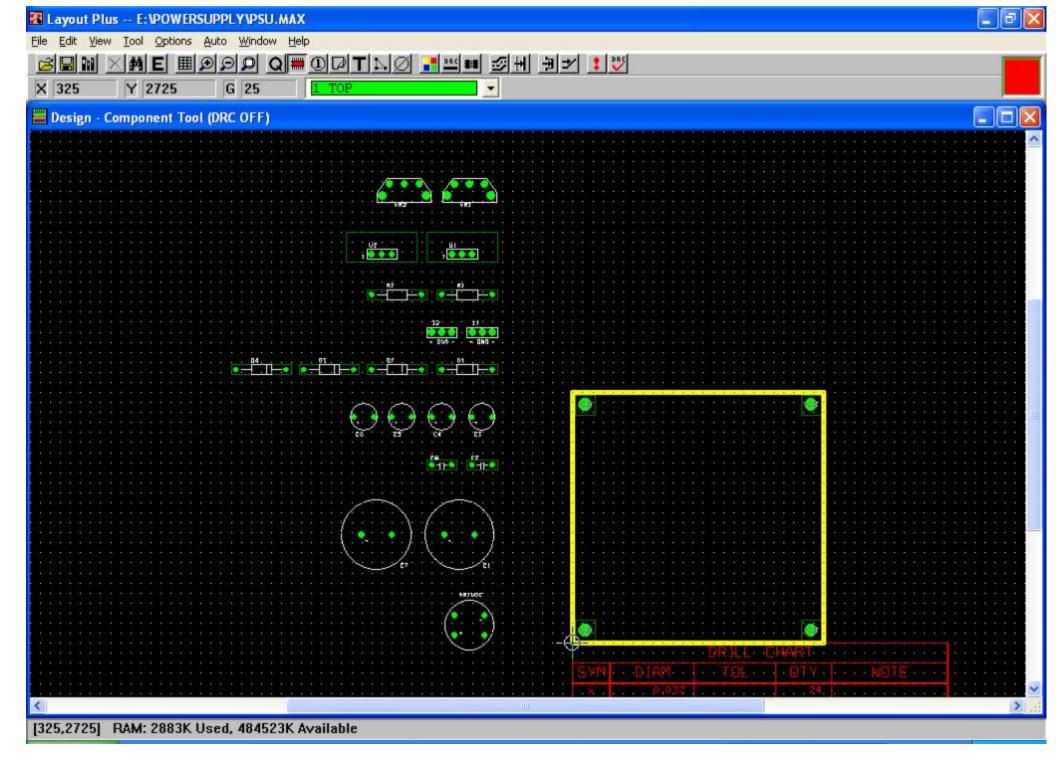


Edit Component	
<u>R</u> eference Designator	MH1
Part Type	0
⊻alue	0
Eootprint BOARD	MOUNTING HOLE
Location X 100. Y 100.	<u>R</u> otation 0
<u>G</u> roup # 0 Component flags	Cl <u>u</u> ster ID
□ Fixed □ Locked □ Non-Electric □ Route	I <u>K</u> ey Enabled <u>D</u> o Not Rename
	Help <u>Cancel</u>

Give this component a reference designator of **MH1**. Then click the **Footprint** button and select the **BOARD MOUNTING HOLE** footprint from **PSU_FOOTPRINTS** library. Check the **Non-Electric** checkbox so that it becomes checked with a dark tick and uncheck the **Route Enabled** checkbox since this is a non-electrical part. Click **OK** when finished. The part will now be attached to your cursor and you can place it on the board. Place it at the edge of the board in the lower left corner.



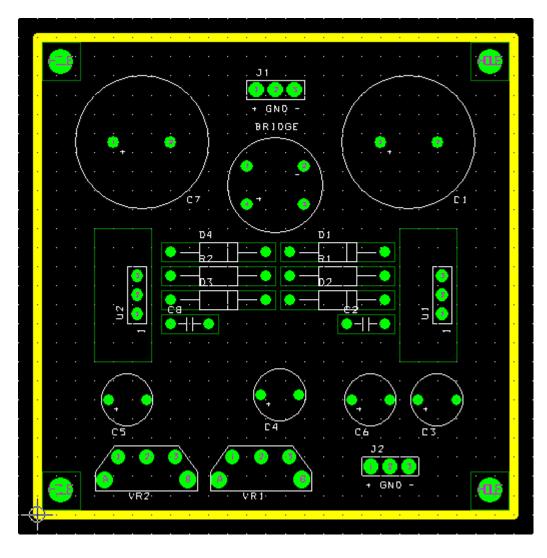
We want to place a mounting hole in each corner of the board. Highlight the **MH1** you just placed and press **CTRL+C**. Place the new mounting hole at the lower right corner. Copy the hole again and complete the four corners. If we don't want to get these mounting holes accidentally moved, then it is possible. Open the **Components** spreadsheet and highlight **MH1 – MH4**. Press **CTRL+E** and re-check the boxes labeled **Fixed** and **Locked**. All the four mounting holes are now fixed and locked at their places. Press **SHIFT+Home** and your board should be in a condition like this.



Now you can begin to place the rest of your components. You will probably want to open up your schematic in Capture so that you can see where the components are supposed to go in relation to each other. For a greater ease, you can print your schematic page out. When you pick up a component, the

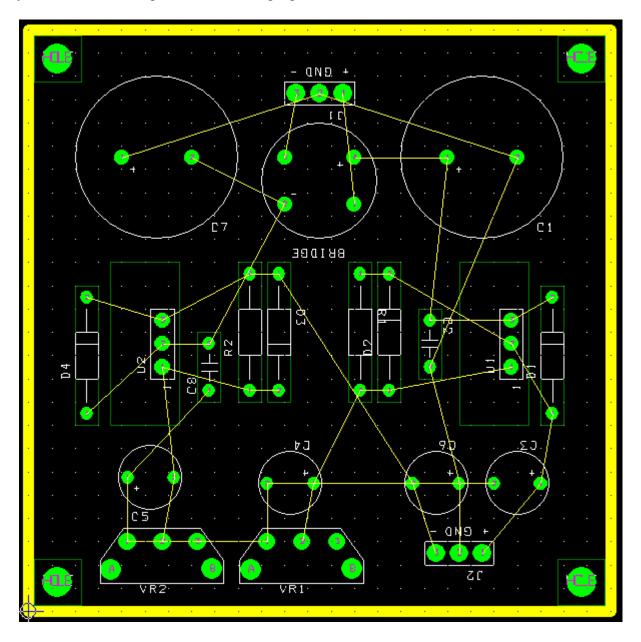
ratsnest for that component will appear to show you the connections to other parts. If you want, you can also turn the ratsnest back on to see all of the nets or some specific nets. To select all the nets, click the **Net Name** header and to select some of the nets, hold down the **CTRL** key while selecting the nets. Press **CTRL+E** and in the dialog that appears, re-check the box labeled **Routing Enabled.** Right now, don't display any of the nets.

Always place those components first, which have the interface at the front or the rare panel. In this design **VR1**, **VR2** have the interface on the front panel. Place them at the lower left corner of the board. Then place the **J1** and **J2** power connectors on the upper middle and lower right of the board respectively, the **bridge** below J1 and the two large **capacitors** beside the bridge. Try to keep components that belong together near each other. Place the remaining parts on the board. When you are done, your board should look something like this.



Now we will improve the placement of our parts. For this, turn all the ratsnest visible. The ratsnest will assist you in placing and rotating the parts efficiently. Place the components in such a location that the ratsnest shows the minimum mess. This way, you will be able to route the board easily. Use **R** key to rotate the parts and try to place them according to figure below. The screen gets too messy when you work while the ratsnest in visible. Use the **Refresh All**

button to refresh the display and the **M** key to redraw the ratsnest and to minimize the connecting wires of the ratsnest. When you are done, you should have your board something like the following figure.



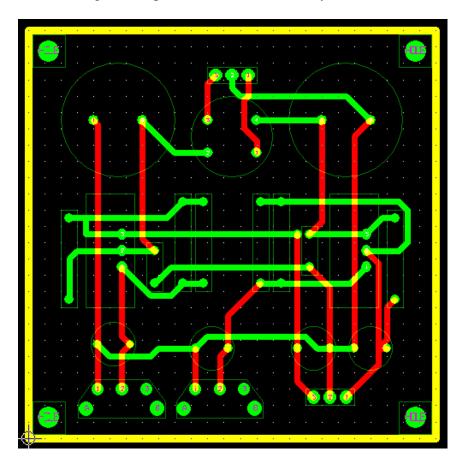
Save your design. You may get the following warning. Ignore it. It is due to the mounting holes that we added.



Now we will route the board. The silkscreen looks a bit messy, but we will deal with that later. In fact, during routing, the silkscreen can get in the way; so turn the **SST** layer invisible now. There are two ways to route a board - Autorouting and Manual Routing

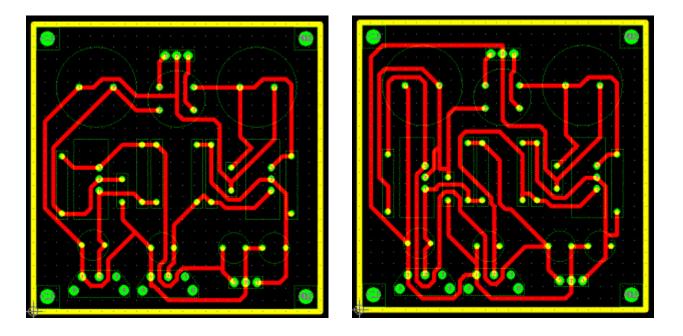
9.3 Autorouting

To let the Layout automatically route the board for you, select Auto->Autoroute->Board. In a second or two, Layout will route the whole board. Click OK at the message. Then press SHIFT+Home and your board should look like this.

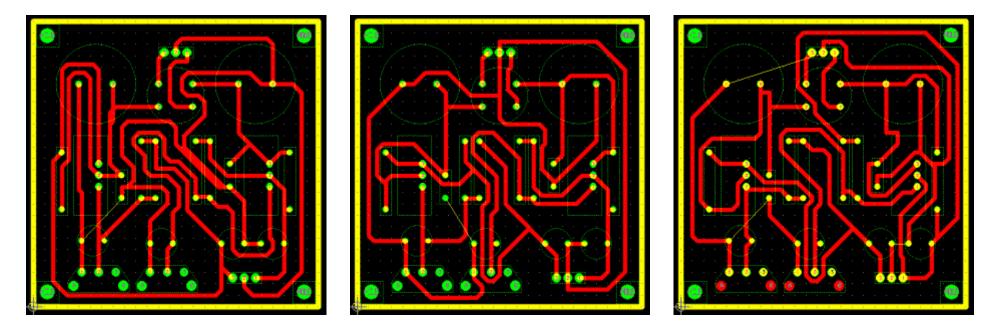


You will certainly never get the exact pattern of copper tracks as shown above. This is because Layout routes the board in a random manner. Every time you autoroute the board, you will get a different conductor pattern. To confirm this fact, select Auto \rightarrow Unroute \rightarrow Board to unroute your board and then again autoroute. Repeat this procedure until you are satisfied with the pattern.

We have routed the board on both the top and bottom layers using the autorouter. But this design is too less dense to justify the routing on both sides. Routing on both the layers increases the cost of your board. In fact designs much more denser than this, are routed on single layer as far as possible. So go ahead and unroute the board first. Open the **Layers** spreadsheet, highlight the **TOP** and **SMTOP** layer and press **CTRL+E** to bring up the **Edit Layer** dialog. Select **Unused Routing** radio button and click **OK**. We have turned **SMTOP** layer off because there is no need for it in the absence of copper tracks on the **TOP** layer. Now our board will contain parts on the top side and copper tracks on the bottom side. After these layer settings, autoroute the board again. This time Layout takes a while to finish its job. Here are two samples of what autorouter did at my computer.



You must notice that autorouter did not route the board well in the second figure. The tracks are longer than necessary and look like a maze. Even worse, autorouter sometimes leaves 1 or 2 connections unrouted. This can be seen in the following figures. The yellow line indicates the unrouted connections.

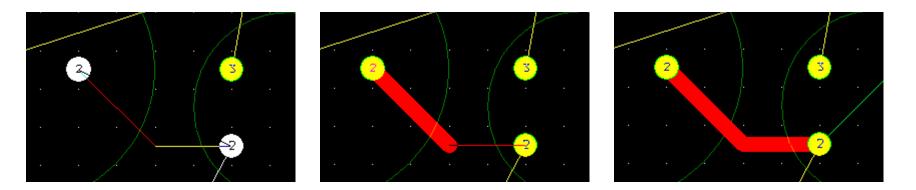


These samples indicate that you should not rely completely on autorouter. Also it cannot differentiate between ordinary nets and critical nets and routes the critical nets in the same haphazard manner. Critical nets like clocks, RF, VHF and UHF signals, etc. should be routed with the shortest possible tracks and require special attention. So you should be also competent at manual routing. In fact all the professional designs or at least the critical nets in a design are routed manually and little help is taken from autorouter. Next I will demonstrate you, how to manually route a board.

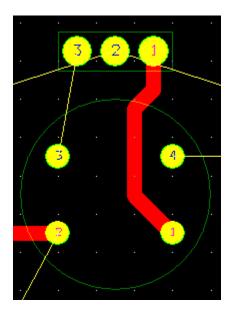
9.4 Manual Routing

Unroute the board by selecting Auto \rightarrow Unroute \rightarrow Board. Now that the board is completely unrouted, you can start manual routing. Press M so that the ratsnest shows you the minimum possible connections. This will help you greatly in the routing process. First we will route on both sides. So activate the **TOP** and **SMTOP** layers in the same way you turned them off. Declare the **TOP** as **Routing Layer** and **SMTOP** as **Documentation** layer in the **Edit** Layer dialog box. Also activate \square **Online DRC.** The box with the dashed line will appear. While DRC is on, you will only be able to place tracks inside this box, but Layout will also block your cursor to route a track in a location where any spacing errors occur. You can resize the DRC box by pressing 'B' and drawing a new rectangle. Enclose the whole board in the DRC box now. **Online DRC** ensures that routing is done in accordance with the DRC. DRC also include the settings that you specified in the **Route Spacing** dialog box (select **Options** \rightarrow **Global Spacing**) in your template.

Let's route a connection. Turn on the **Edit Segment Mode** or **Add/Edit Route Mode** $\exists \exists d$. The two have some subtle differences. Experiment with both to see which one you are most comfortable with. I recommend you to start with the **Edit Segment Mode**. Start by routing the connection that is between the pin 2 of bridge and pin 2 of capacitor on its left. Zoom in a bit and click on the ratsnest near pin 2 of the capacitor. You will see a thin green line attached to your cursor which shows the path of the copper track that will be routed. We want to place this track on the bottom layer so press 2 to switch to the bottom layer. The green line will turn red; the colour of the bottom layer. Left-click to place a segment of a track. When you get near to pin 2 of the bridge, you can press **F** to have Layout finish the track for you.



When routing you will want to redraw the ratsnests occasionally (press \mathbf{M}). Now route the following connection. It has 4 segments and 3 bends. Start by clicking at the ratsnest near one of the pins, click once for each bend and press \mathbf{F} to finish the track. You can also click at the pin to finish the track instead of pressing \mathbf{F} .



Here is a list of hotkeys that you will find very useful during routing.

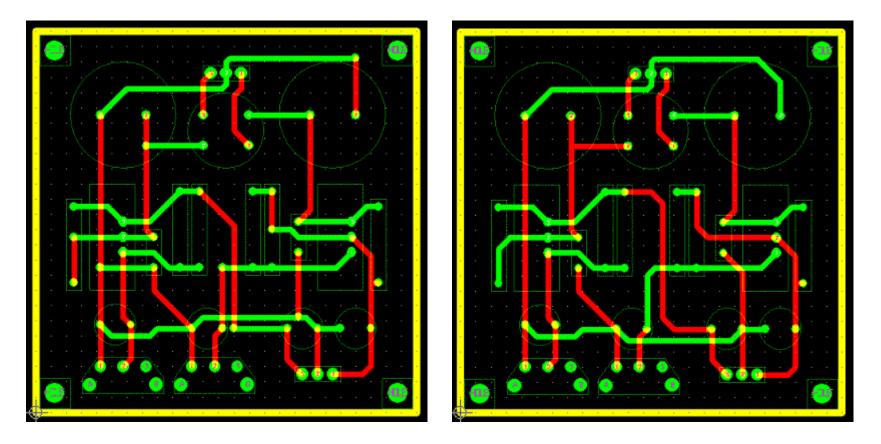
- F auto-complete a connection
- G unroute a segment
- D unroute a connection
- Alt+D unroute a whole net
- V add via
- 1,2 switch to top and bottom layer respectively
- U undo (only one step undo is possible)

If you are routing a connection and have routed a wrong segment, press G and the previous segment will be unrouted. If you are not between routing a connection, just move your cursor over a segment and press G. The segment will be unrouted.

Go on routing the board. If you are unable to route a connection on a layer, switch the layer and route the connection on that layer. If the connection still cannot be routed on the other layer then use the following technique to route a connection using both layers. Press V to add via and then switch the layer by pressing 1 or 2. Now complete the connection. More than one vias can be used in connection but remember! Vias increases the cost of your board. So avoid using too much vias. If possible keep one connection at one layer only.

IMPORTANT NOTE: It is a good design practice to keep routes on one layer oriented in the same direction. For example, you might want to have all tracks on the top layer oriented horizontally, while all routes on the bottom are oriented vertically. Doing this increases the number of vias that are needed, but makes routing much easier, especially in very dense designs. After routing is complete, you can go back and remove unnecessary vias. Of course, sometimes it will be impossible to adhere to this guideline.

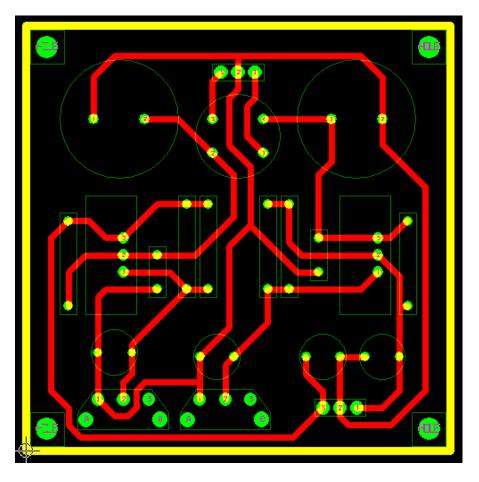
You will indeed feel some difficulty while routing in the beginning but as you practice, you will enjoy it and prefer to route your every board manually. Complete the routing now. The figure below shows the routing that I had done. Notice there are 7 vias in first figure (can you identify them all?). All of them are redundant and are used to comply with the design strategy that is mentioned above. In the second figure, all of them are removed.



Let's look a little bit at some of the tools that Layout gives you to check on the progress of your design. Click the **View Spreadsheets** icon and choose **Statistics**. The statistics spreadsheet gives you information on time in layout, percent of components placed, percent of tracks routed, and some other

information. It also tells you how many vias you have used in your board. If there remains no ratsnest on the board and the **Statistics** spreadsheet also shows the % **Routed** as 100%, it means that you have done all the routing.

Unroute the board because we are now going to route on single side only. Make sure that **Online DRC** is activated and turn off **TOP** and **SMTOP** layers. Start routing in the similar fashion, but this time there is no top layer to provide you an alternate way to run the tracks over the existing tracks without shorting them. So it is your ingenuity how you tackle such a situation. Route the initial connections in such a way so as to leave enough room for later connections. Sometimes you will have to delete the existing tracks to provide path for other tracks and then re-route the deleted connections through some another way. It will often happen to you that you will have completed all routing except one or two connections and will be unable to find a path to route them. Try moving some parts to a new location to make room for the remaining connections. Follow these guidelines and route all the connections. The figure below shows how I had done the job.



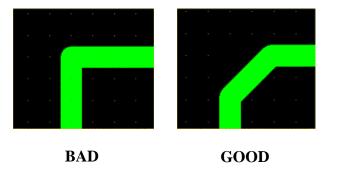
Compare this manual routing with autorouting. You can easily appreciate the difference between human intelligence and artificial intelligence.

9.5 Cleaning up the Design

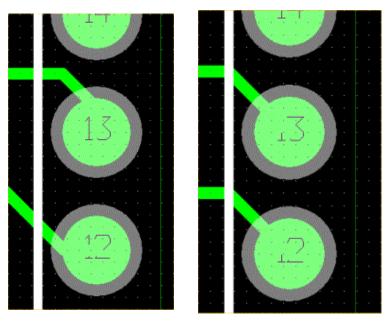
Now it is time to clean up your design. You should think of your board as a work of art. Other people may look at it, so you want it to look nice. Furthermore, a clean design will ensure fabrication success. When cleaning the design, the following should be kept in mind.

A. Route Spacing – You have set a minimum of 15 mils for track-to-track spacing in your design. However, do not pack tracks closely together unless you have to. Routing tracks closely is generally a bad idea because this can result in undesired capacitive and inductive effects between tracks.

B. Right Angles in Tracks – Don't use right angles in routing your tracks. Chamfer the corners.



C. Pad Exits – Track exits from pads should be clean and not come out of the pad at unusual angles.

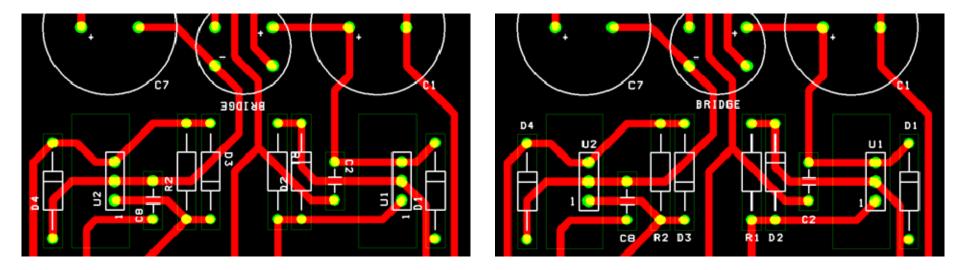


BAD

GOOD

D. Remove Extra Vias – Vias add cost to a board, so it is a good practice to remove any unnecessary vias from your design

E. An Orderly Silkscreen – Make the **SSTOP** layer visible and use the **Text Tool** to adjust the silkscreen. Rotate the inverted text, move the text to a suitable location. All text should be oriented in the same direction for readability. Silkscreen cannot overlap pads or vias (overlapping tracks is OK). Change the **Detail Grid** to a finer setting if necessary. Reference designators should be placed as close to the part as possible. Polarity signs and pin number should be placed in the correct position.



BAD

GOOD

9.6 Documenting the Design

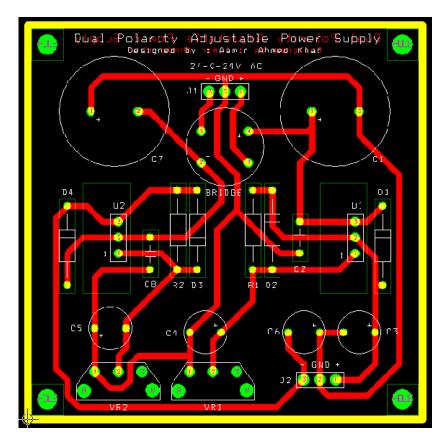
Good documentation of your design will help both in manufacturing and debug. First, we can add some useful text to the silkscreen. For example, the **J1** power connector is connected to the secondary of $240V \rightarrow 24-0-24V$ transformer. Maybe you want to put some text on the board to indicate that. You can use the **Text Tool** to create new text. Right-click anywhere in the design and select **New...** to get the **Text Edit** dialog.

Text Edit								
Text 75								
Type of Text	Type of Text							
<u>T</u> ext Stri	ng 24-0	-24V AC						
Image: Eree C Lustom Properties Image: Eree C Lustom Properties Image: Eree Package Name Image: Eree Footprint Name								
	Text location [1020.,2390.]							
Line Width 8.	•	Text Height	50					
Rotat <u>i</u> on 0		Char <u>R</u> ot	0					
Radiu <u>s</u> 0.	•:	Char Asp <u>e</u> ct	100					
☐ <u>M</u> irrored								
Layer:								
Comp <u>A</u> ttachment								
OK <u>H</u> elp <u>C</u> ancel								

Most text you create will be **Free**. For good readability, I suggest a **Line Width** of 8 and a **Text Height** of 50 to 75. A 6 mil **Line Width** is about as small as you can go to keep the text readable. One very useful thing is to add some information about the board, as well as the initials of the person who designed it. Place this information on **SSTOP** as well as **BOT** layer. It will look nice to have the title and your name on the board in copper trace. Remember to mirror (**Ctrl+M**) any text that you put on bottom layer. If you are unable to find enough room on the bottom layer to place the text, then put it on silkscreen only. Placing the text at bottom layer on tracks can short the tracks. Place some text like the figure below.



Congratulations! Your board design is now finally complete. Here is the completed board.



10. Archiving Your Design

The final thing you should do is a little file cleanup in your directory hierarchy. Orcad generates a lot of files that you don't really need to keep. Below is a list of the files you need to keep in each directory. You can safely delete all the others.

- schematic*.opj - Capture project file .
 - schematic*.dsn - Capture design file
 - schematic*.mnl - Layout netlist file - Layout board file (You don't need to keep the backup files)
- board*.max •

•

- libraries*.olb - Capture library file
- libraries*.llb - Layout library file
- libraries*.tpl - Layout template file •

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