SIEMENS

Corporate Technology

Siemens SRL, Romania

TRANSILVANIA University of BRAŞOV

Faculty of Electrical Engineering and Computer Science

Department of Electronics and Computers

Low Noise, Low Power Variable Gain Amplifier for Ultrasounds

Adrian-Virgil CRĂCIUN

Joint International Conference OPTIM – ACEMP 2017

Optimization of Electrical & Electronic Equipment

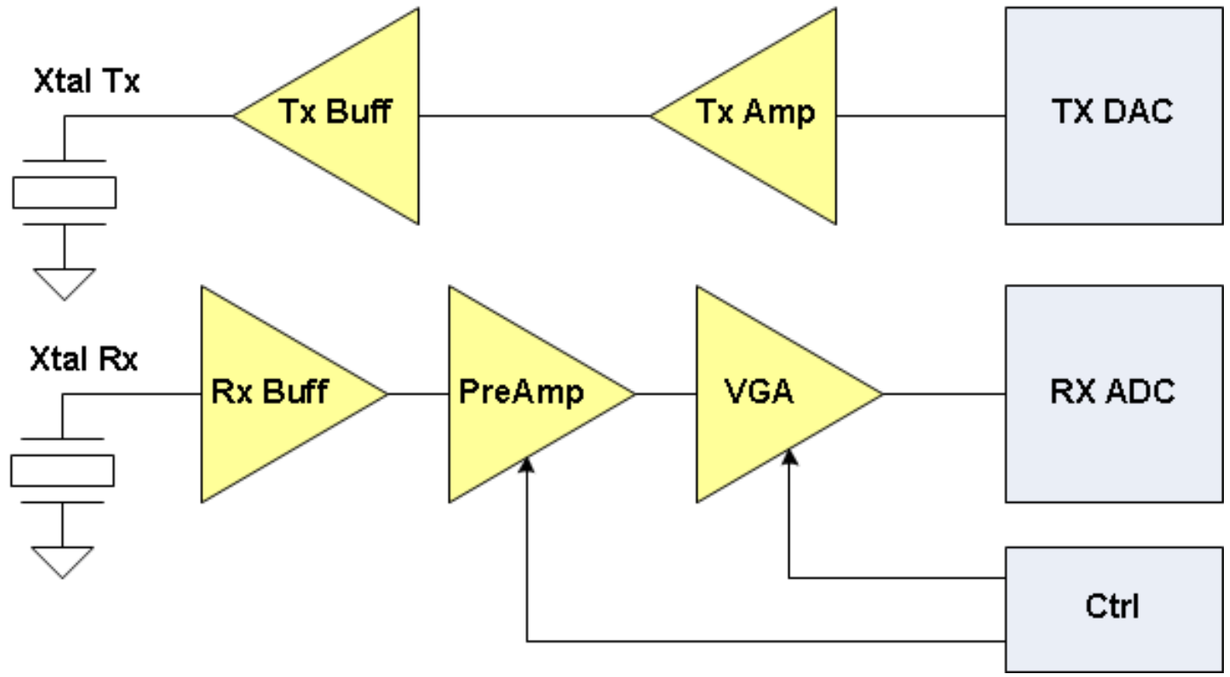
Aegean Conference on Electrical Machines and Power Electronics

May 25-27, 2017, Brașov, Moieciu-Fundata ”Cheile Grădiștei”

General presentation

- This paper presents the simulation of a variable gain amplifier from three perspectives:
  - functional, using LTspice circuit simulator;
  - signal-to-noise-ratio, computed with Excel and
  - power consumption, estimated with ACEplorer power simulator.
- The architectural decisions are taken based on these simulations to meet the requirements:
  - a dynamic range greater than 60 dB;
  - a frequency domain of 100 kHz to 3 MHz;
  - power consumption lower than 20 mW and
  - the signal to noise ratio greater than 12 dB (for an input sensitivity better than 50 microvolts).

- The analog part of the portable ultrasonic measurement systems consists on a transmission (TX) chain and a receiver (RX) chain.
- The delay between TX and RX signal is measured; to have good results the output of TX chain (with a peak voltage of 13 V) is send also to the input of RX chain. The voltage range at the preamplifier input will be from tens of microvolts to volts (5 decade);



Symplified Block diagram of the system

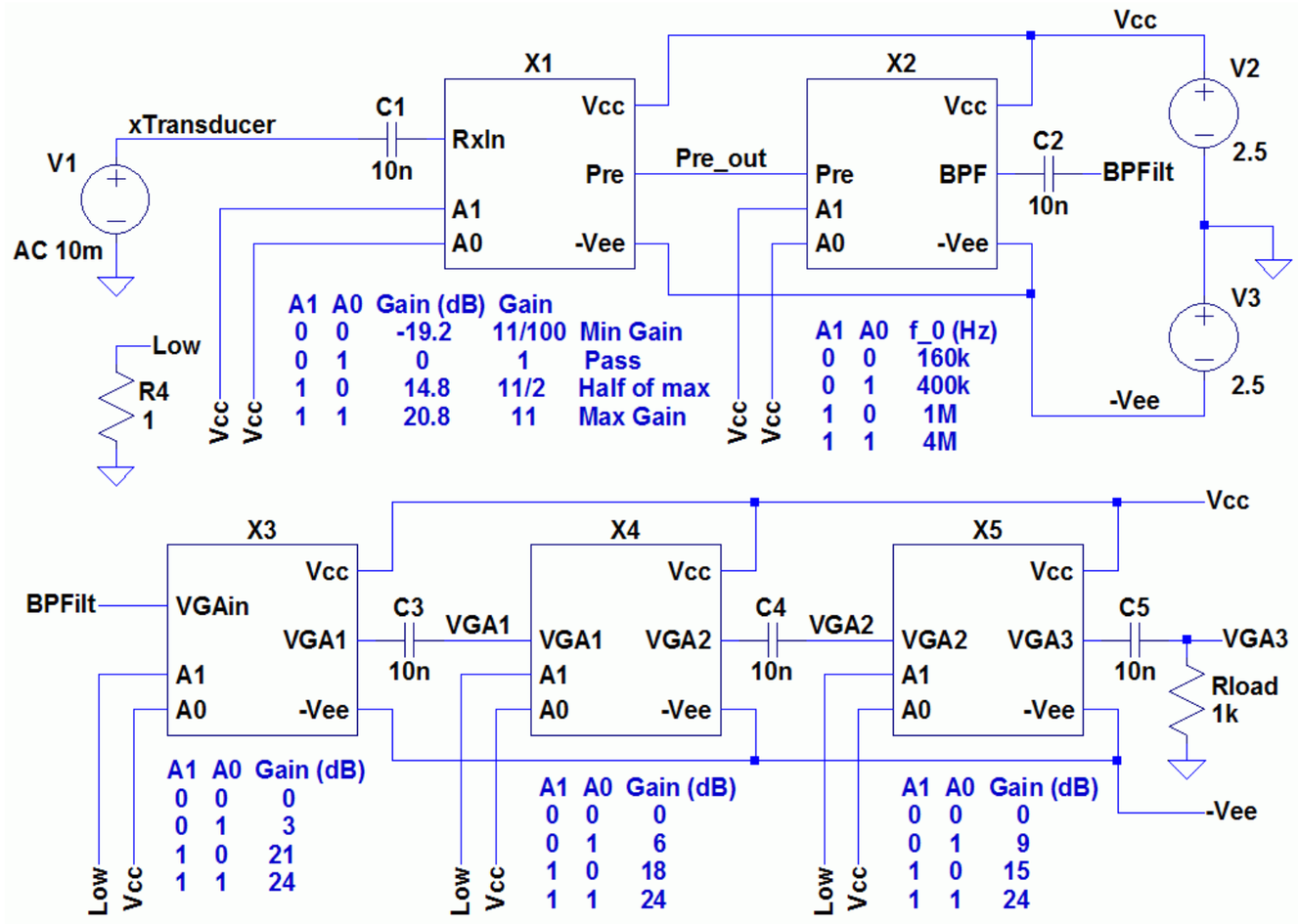
The RX Variable Gain Amplifier

• The preliminary architecture presented in figure consists on: the buffer, the preamplifier and the VGA; three stages VGA has been considered with a gain of 0 to 24 dB each; that gives a gain variation of 72 dB (3x24); an additional requirement is to vary the gain in steps of 3 dB to use more than 70% of the ADC range. A possible allocation of gains for the 3 stages is:

- 24 / 15 / 9 / 0 dB for one stage;
- 24 / 18 / 6 / 0 dB for another stage;
- 24 / 21 / 3 / 0 dB for the other stage.

• The preamplifier gain should be greater than 11 dB (for the minimum sensitivity of 50 microvolts) and the attenuation (for the maximum input of 10 V) should be less than -23 dB. The preliminary preamplifier gains (and attenuations) are:

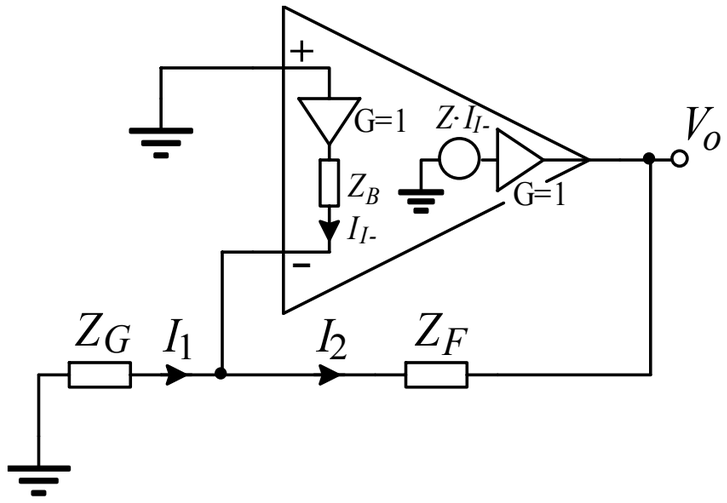
- 12 / 6 / -9 / -24 dB; the two intermediate values can be modified according to other possible needs.



Block diagram of the RX amplifier

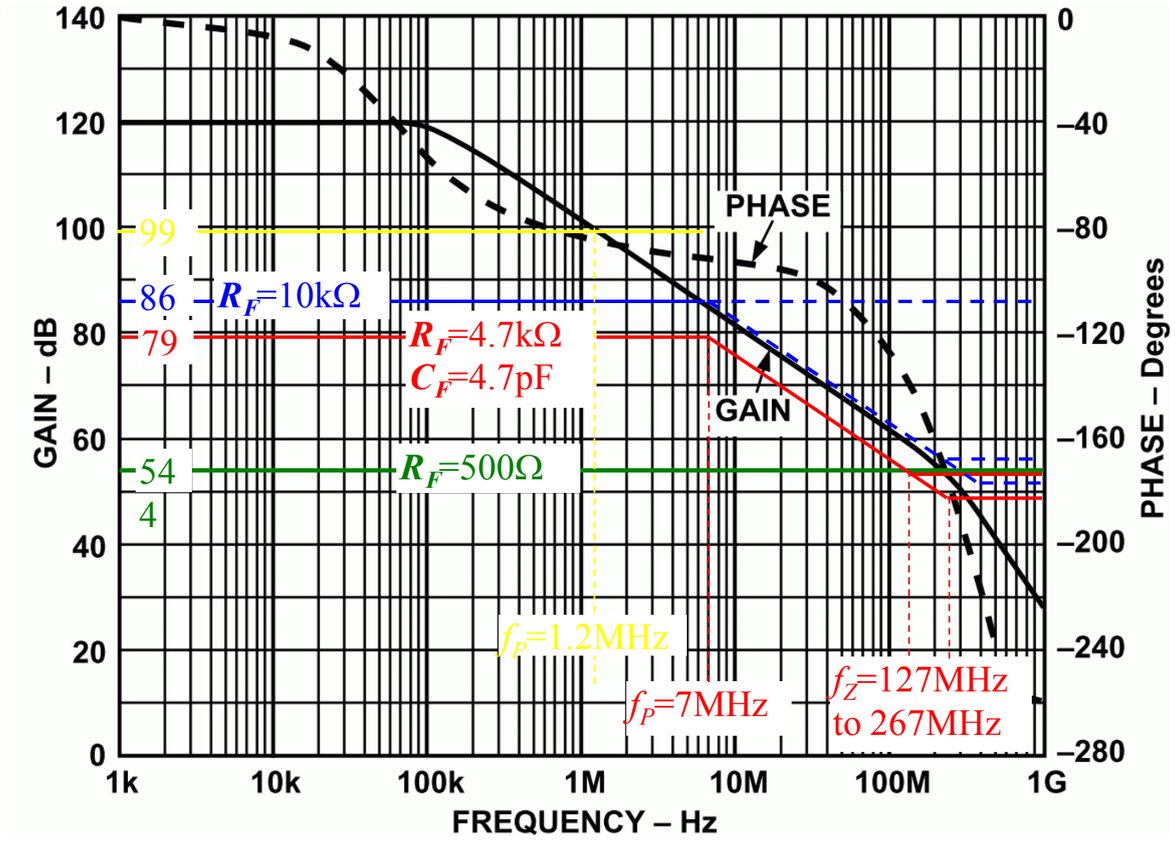
Stability of CFA

The circuit used to analyze the stability is presented in the next figure. The signal injection point is not relevant from the stability point of view; the input was grounded.



The stability has been evaluated at the point of intersection of the open-loop gain (*Z*) with the ideal closed-loop gain (1/b) – 0dB point of the loop gain.

The feedback impedance used by inverting configuration consists on a 4.7kΩ resistor in parallel with a 4.7 pF capacitor, used to filter the alias frequency – red line in the figure.



Graphical stability analysis realized on the gain-frequency CFA characteristic (ADG8005)

With the 4.7 kΩ feedback resistor and with the minimum gain case, the filtering frequency will be of 1.2 MHz; at the intersections of an equivalent 1/b value of 99dBΩ (79dBΩ + 20dBΩ) with the open-loop characteristic – yellow line.

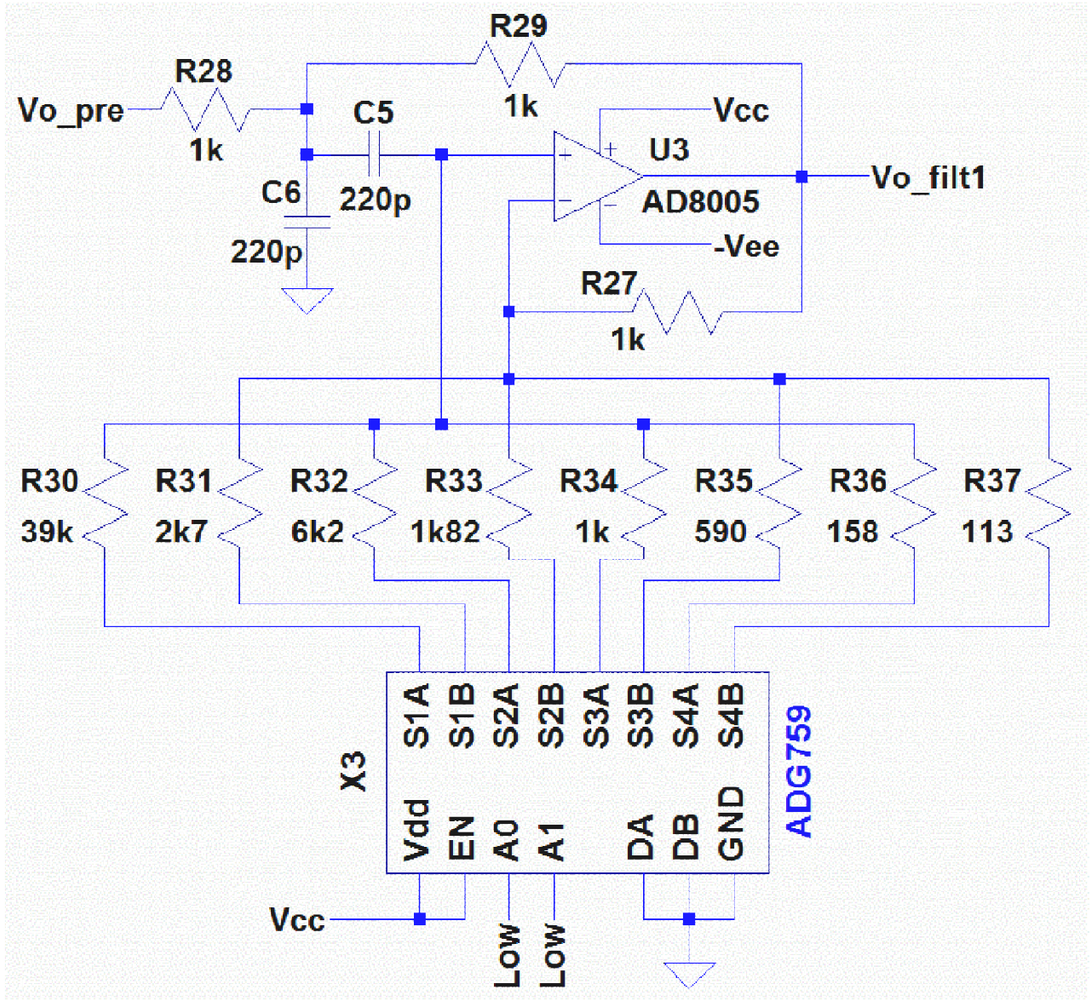
Based on these analyses a separate filter (instead of *CF*) would be a good alternative.

Limiting of Bandwidth

Filters are used to reduce the bandwidth (*BW*); that will reduce the input noise and increase the signal-to-noise ratio. In this analysis a switchable filters is proposed.

A KRC (Salen-Key) active filter is considered since it does not require reactive elements in the (negative) feedback path, which would compromise stability of CFA.

A solution for the filter was calculated to cover the frequency domain with 4 set of values and with a gain of 6 dB at the center frequency of the filter. The low and high frequency were estimated with a quality factor of 1. Simulation and theoretical results are compared in next table.



Simulation circuit for the 2nd order active filter with MUX

Theoretical and simulation results for 3 set of values

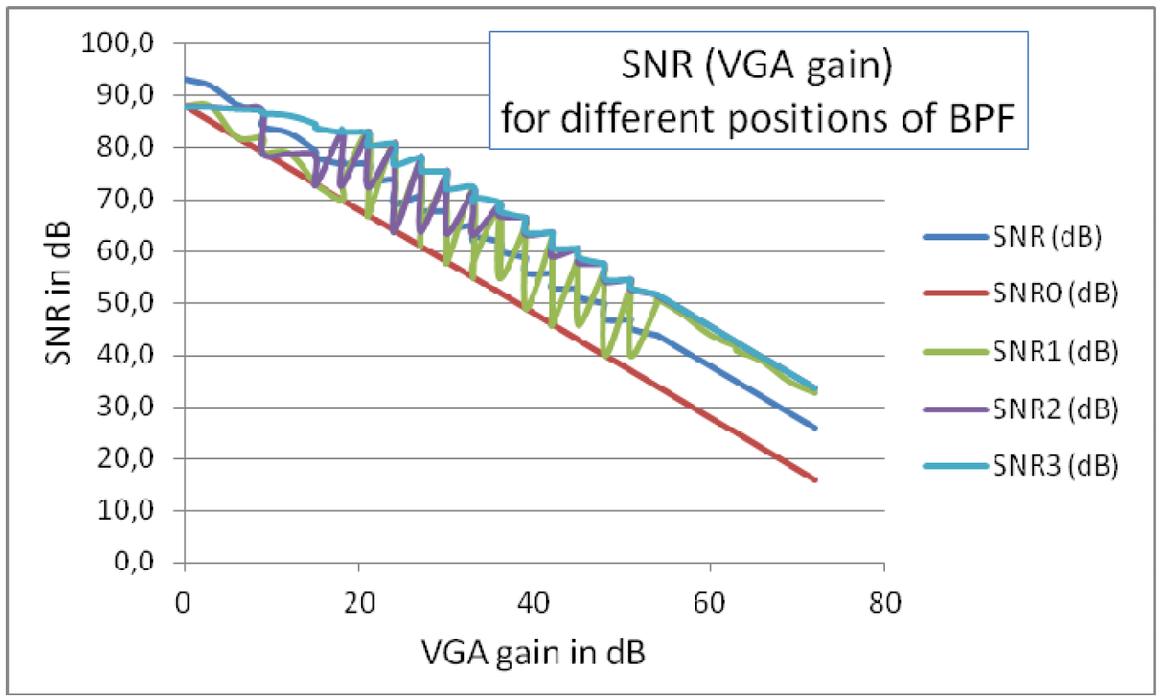
	Th	Sim	Th	Sim	Th	Sim
f0 (MHz)	1	1	2	1.99	0.5	0.5
R3 (Ω)	1k	1k	250	249	4k	4020
K0	2.67	-	6.67	-	1.67	-
***RG* (Ω)**	600	590	176	124	1.5k	1500
Q	1.06	1.06	0.85	0.9	0.85	0.82
H0 (dB)	6.0	6.1	6.0	6.06	6.0	5.8
BW (MHz)	0.94	0.94	2.36	2.2	0.59	0.61

The analog MUX effect is the reduction of the gain (*H0*) at the central frequency when filter frequency decrease. This effect was compensated by adjusting the component values and verify by simulation.

Signal to Noise Ratio Analysis

The RX buffer and preamplifier determine the input noise and the SNR of the whole circuit. To get a good SNR, the buffer circuit is realized with low noise transistors and the preamplifier circuit is realized with the low noise AD8014 CFA. The band pass filter (BPF) position influences the noise.

The results of the Excel noise model for the lower bandwidth (BW) of the BPF are presented in next figure.

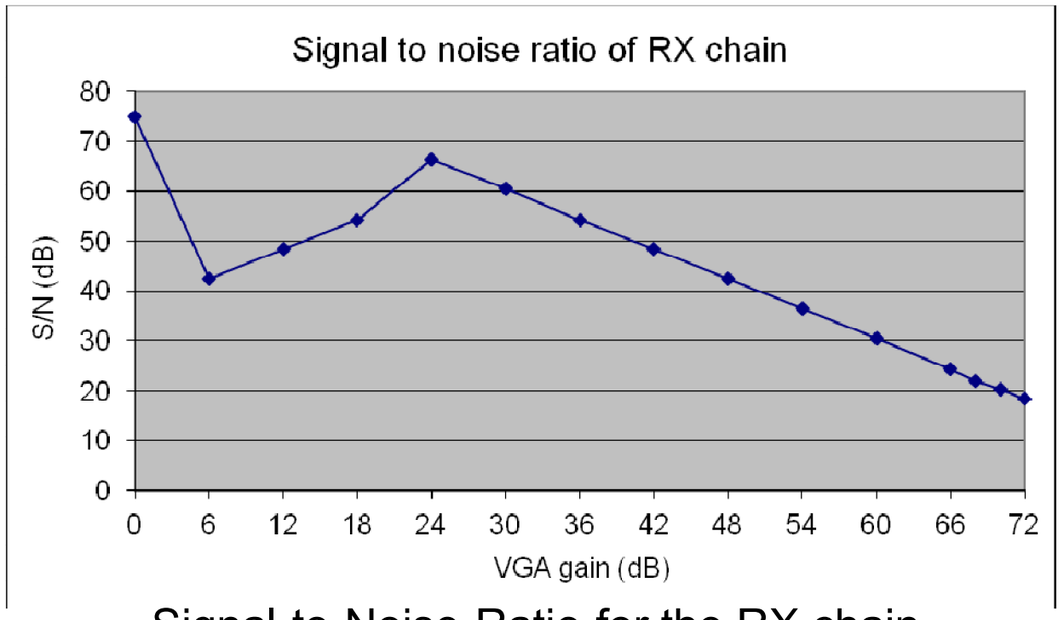


Signal-to-Noise-Ratio for different positions of BPF

The worst cases are with the BPF at the input of the circuit and without BPF. The best case, for all VGA gains, is with the BPF after the VGA.

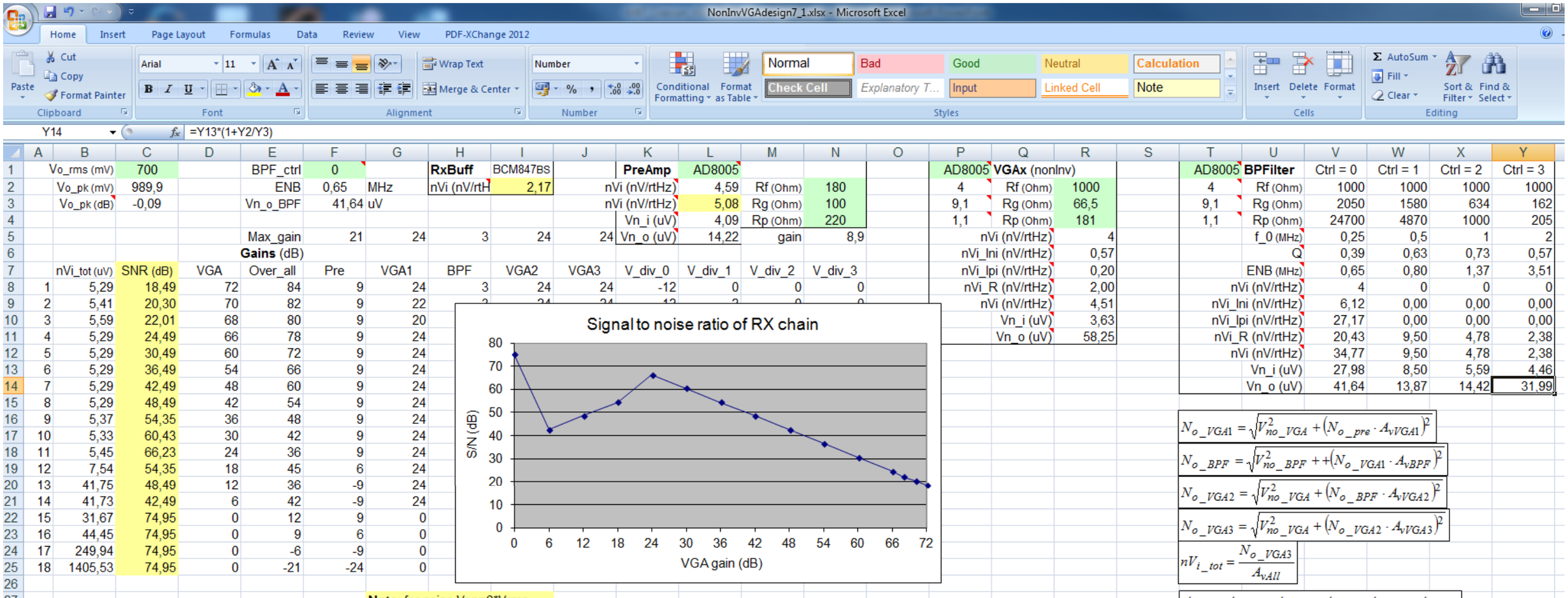
The whole RX chain is modeled in Excel; it contains the actual circuits with the buffer, the preamplifier, the VGA and the BPF.

The simulation results presented in figure are with the BPF set at the 1st position (with a BW of 0.65 MHz). At the center frequency of the BPF, the input sensitivity is 45 micro-volts, with a corresponding SNR of 18.5 dB.



Signal-to-Noise-Ratio for the RX chain

Signal to Noise Ratio Computing



	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y
1		Vo_rms (mV)	700		BPF_ctrl	0		**RxBuff**	BCM847BS		**PreAmp**	AD8005				AD8005	**VGAx** (nonInv)			AD8005	**BPFilter**	Ctrl = 0	Ctrl = 1	Ctrl = 2	Ctrl = 3
2		Vo_pk (mV)	989,9		ENB	0,65	MHz	nVi (nV/rtH	2,17		nVi (nV/rtHz)	4,59	Rf (Ohm)	180		4	Rf (Ohm)	1000		4	Rf (Ohm)	1000	1000	1000	1000
3		Vo_pk (dB)	-0,09		Vn_o_BPF	41,64	uV				nVi (nV/rtHz)	5,08	Rg (Ohm)	100		9,1	Rg (Ohm)	66,5		9,1	Rg (Ohm)	2050	1580	634	162
4											Vn_i (uV)	4,09	Rp (Ohm)	220		1,1	Rp (Ohm)	181		1,1	Rp (Ohm)	24700	4870	1000	205
5					Max_gain	21	24	3	24	24	Vn_o (uV)	14,22	gain	8,9			nVi (nV/rtHz)	4			f_0 (MHz)	0,25	0,5	1	2
6					**Gains** (dB)												nVi_Ini (nV/rtHz)	0,57			Q	0,39	0,63	0,73	0,57
7		nVi_tot (uV)	SNR (dB)	VGA	Over_all	Pre	VGA1	BPF	VGA2	VGA3	V_div_0	V_div_1	V_div_2	V_div_3			nVi_Ipi (nV/rtHz)	0,20			ENB (MHz)	0,65	0,80	1,37	3,51
8	1	5,29	18,49	72	84	9	24	3	24	24	-12	0	0	0			nVi_R (nV/rtHz)	2,00			nVi (nV/rtHz)	4	0	0	0
9	2	5,41	20,30	70	82	9	22										nVi (nV/rtHz)	4,51			nVi_Ini (nV/rtHz)	6,12	0,00	0,00	0,00
10	3	5,59	22,01	68	80	9	20										Vn_i (uV)	3,63			nVi_Ipi (nV/rtHz)	27,17	0,00	0,00	0,00
11	4	5,29	24,49	66	78	9	24										Vn_o (uV)	58,25			nVi_R (nV/rtHz)	20,43	9,50	4,78	2,38
12	5	5,29	30,49	60	72	9	24														nVi (nV/rtHz)	34,77	9,50	4,78	2,38
13	6	5,29	36,49	54	66	9	24														Vn_i (uV)	27,98	8,50	5,59	4,46
14	7	5,29	42,49	48	60	9	24														Vn_o (uV)	41,64	13,87	14,42	31,99
15	8	5,29	48,49	42	54	9	24																		
16	9	5,37	54,35	36	48	9	24																		
17	10	5,33	60,43	30	42	9	24																		
18	11	5,45	66,23	24	36	9	24																		
19	12	7,54	54,35	18	45	6	24																		
20	13	41,75	48,49	12	36	-9	24																		
21	14	41,73	42,49	6	42	-9	24																		
22	15	31,67	74,95	0	12	9	0																		
23	16	44,45	74,95	0	9	6	0																		
24	17	249,94	74,95	0	-6	-9	0																		
25	18	1405,53	74,95	0	-21	-24	0																		
26																									
27							**Note**: for noise Vpp=6*Vrms																		
28					**Gains**																				
29		V_in		VGA	Over_all	Pre	Vo_Pre (pp)	VGA1	BPF	VGA2	VGA3	S/N Pre_o	Vo_VGA1	No_VGA1	S/N VGA1	Vo_BPF	No_BPF	S/N_BPF	Vo_VGA2	No_VGA2	S/N VGA2	Vo_VGA3	No_VGA3	S/N VGA3	Vo_pp
30	1	44,46	uV	3981	15746	2,80	0,35	15,85	1,41	15,85	15,85	8,75	1,97	233	8,47	2,79	331	8,41	44	5,25	8,4	700	83,26	8,41	1980
31	2	55,97	uV	3162	12507	2,80	0,44	12,59	1,41	15,85	15,85	11,02	1,97	188	10,48	2,79	269	10,35	44	4,27	10,4	700	67,62	10,35	
32	3	70,46	uV	2512	9935	2,80	0,56	10,00	1,41	15,85	15,85	13,87	1,97	154	12,84	2,79	221	12,61	44	3,50	12,6	700	55,53	12,61	
33	4	88,70	uV	1995	7891	2,80	0,70	15,85	1,41	15,85	7,94	17,47	3,94	233	16,91	5,56	331	16,78	88	5,25	16,8	700	41,73	16,77	
34	5	176,99	uV	1000	3955	2,80	1,40	15,85	1,41	15,85	3,98	34,85	7,85	233	33,74	11,1	331	33,47	176	5,25	33,5	700	20,91	33,47	
35	6	353,13	uV	501	1982	2,80	2,80	15,85	1,41	7,94	3,98	69,5	15,7	233	67,3	22,1	331	66,79	176	2,63	66,8	700	10,48	66,8	
36	7	704,60	uV	251	993	2,80	5,58	15,85	1,41	15,85	1,00	138,7	31,3	233	134,3	44,2	331	133,26	700	5,25	133,2	700	5,25	133,2	
37	8	1405,85	uV	126	498	2,80	11,13	15,85	1,41	7,94	1,00	276,8	62,4	233	268,0	88,1	331	265,88	700	2,63	265,8	700	2,63	265,7	
38	9	2805,05	uV	63,1	250	2,80	22,21	15,85	1,41	1,00	3,98	552,3	124,5	233	534,7	175,8	331	530,50	176	0,34	522,5	700	1,34	522,0	
39	10	5596,80	uV	31,6	125	2,80	44,32	15,85	1,41	2,00	1,00	1102,0	248,4	233	1066,9	350,8	331	1058,49	700	0,66	1054	700	0,67	1050,4	
40	11	11,17	mV	15,8	63	2,80	88,44	15,85	1,41	1,00	1,00	2198,8	495,6	233	2128,8	700,0	331	2111,96	700	0,34	2080	700	0,34	2049,6	
41	12	3,94	mV	7,94	178	2,00	22,21	15,85	1,41	1,00	3,98	552,3	124,5	233	534,7	175,8	331	530,50	176	0,34	522	700	1,34	522,0	
42	13	11,09	mV	3,98	63,1	0,355	11,13	15,85	1,41	7,94	1,00	276,8	62,4	233	268,0	88,1	331	265,88	700	2,63	266	700	2,63	265,7	
43	14	5,56	mV	2,00	125,9	0,355	5,58	15,85	1,41	15,85	1,00	138,7	31,3	233	134,3	44,2	331	133,26	700	5,25	133	700	5,25	133,2	
44	15	176,99	mV	1,00	3,96	2,80	1401,66	1,00	1,41	1,00	1,00	34848	496	60	8265	700	94	7417	700	0,11	6312	700	0,13	5588	
45	16	248,37	mV	1,00	2,818	1,995	1401,66	1,00	1,41	1,00	1,00	34848	496	60	8265	700	94	7417	700	0,11	6312	700	0,13	5588	
46	17	1396,68	mV	1,00	0,501	0,355	1401,66	1,00	1,41	1,00	1,00	34848	496	60	8265	700	94	7417	700	0,11	6312	700	0,13	5588	
47	18	7854,13	mV	1,00	0,089	0,063	1401,66	1,00	1,41	1,00	1,00	34848	496	60	8265	700	94	7417	700	0,11	6312	700	0,13	5588	
48							mV (pk-pk)						mV	uV		mV	uV		mV	mV		mV	mV		
49																									

$$N_{o\_VGA1} = \sqrt{V_{no\_VGA}^2 + \left(N_{o\_pre} \cdot A_{vVGA1}\right)^2}$$

$$N_{o\_BPF} = \sqrt{V_{no\_BPF}^2 + +\left(N_{o\_VGA1} \cdot A_{vBPF}\right)^2}$$

$$N_{o\_VGA2} = \sqrt{V_{no\_VGA}^2 + \left(N_{o\_BPF} \cdot A_{vVGA2}\right)^2}$$

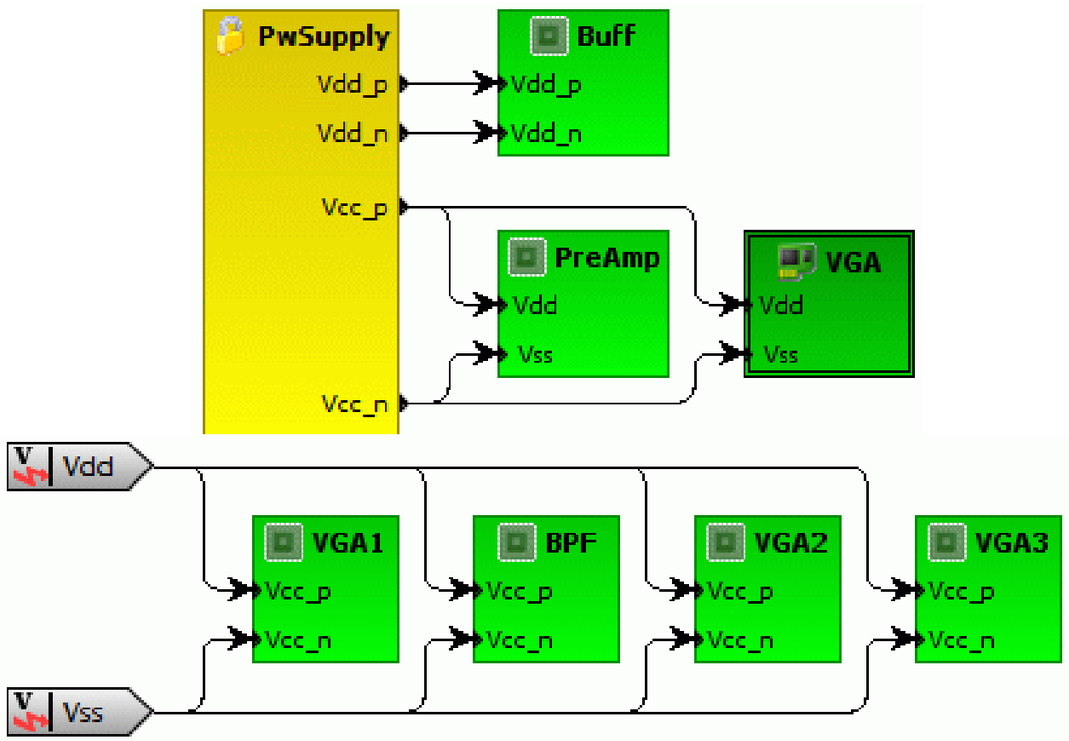
$$N_{o\_VGA3} = \sqrt{V_{no\_VGA}^2 + \left(N_{o\_VGA2} \cdot A_{vVGA3}\right)^2}$$

$$nV_{i\_tot} = \frac{N_{o\_VGA3}}{A_{vAll}}$$

$$A_{vAll} = A_{v\_pre} \cdot A_{vVGA} \cdot A_{vBPF} \cdot A_{vVGA2} \cdot A_{vVGA3}$$

Excel table for computing the Signal-to-Noise-Ratio of the RX chain

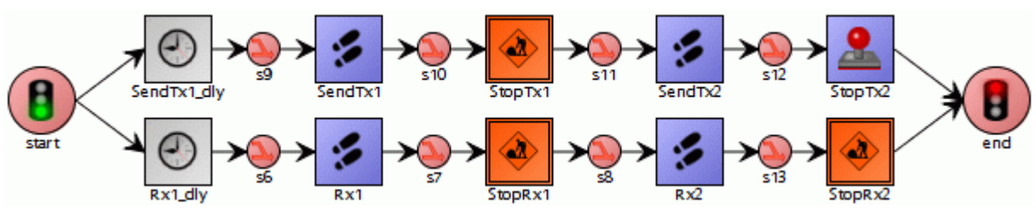
Power Simulation



Block diagram of the RX chain and of the VGA macro-component

The power scenario description is based on the operating use-case that specifies the execution order and timing information.

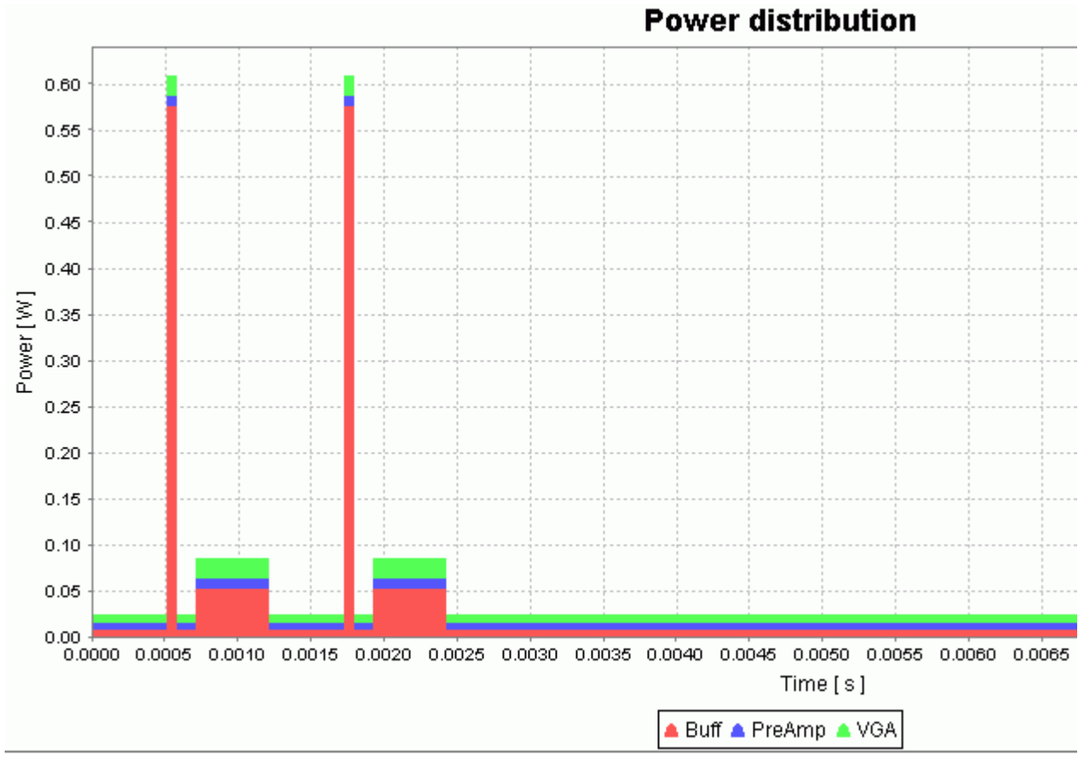
The sequence of operation is periodically executed with a transmission phase of 50 μs and a receiving phase of 0.5 ms.



Scenario description in Aceplorer (a Docea Intel tool)

The scenario was coded with TX activities and RX activities in parallel as indicated in the figure. The scenario elements are the delay (indicate time), the stamp (indicates power states and programmable values), the step (indicates the time and the power operations) and job (a container for other elements).

The average values of VGA part / RX chain for the presented scenario are 11.8 / 36.7 mW (with a minimum of 10.4 / 24.8 mW and a maximum of 22.9 / 609 mW).



Power distribution of RX chain in time

Conclusions

This paper present the architecture and implementation details for an ultrasound variable gain amplifier with low power consumption and low noise for:

- a frequency domain of 100 kHz to 4 MHz,
- a gain variation of 72 dB.
- A signal-to-noise ratio better than 18.5 dB for an input sensitivity of 45 mV;
- Worst case average power consumption is 12 mW

The proposed circuit is realized with low power current feedback amplifiers and consists on:

- a preamplifier with AD8014 with a gain of: -19, 0, 15 and 21 dB,
- a switchable band-pass filter with AD8005 with 6 dB gain and center frequencies of: 0.2, 0.4, 1 and 2.5 MHz,
- 3 VGA stages with AD8005, with a gain of 0 to 24 dB, digitally controlled in 3 dB steps.

The circuit was designed starting from theoretical analysis and was verified by different simulations:

- LT-spice functional simulation,
- Aceplorer, (a Docea Intel tool) used for power simulation,
- Excel estimation and LT-spice noise simulation.

It was analyzed the current feedback amplifier stability. The noise was reduced by limiting the bandwidth with a dedicated switchable filter. The simulation results validate the proposed circuit.

The typical quiescent power consumption is 5 mW for AD8014 and 1.75 mW for AD8005, with a total typical power of about 12 mW; that is lower than the dedicated VGA integrated circuits.