Power Amplifiers

A power amplifier is an amplifier with a high power output stage. In this context, high power means a power greater than 1 W. The output stage usually deals with relatively large signals. Thus, the small-signal approximation and models are either not applicable or must be used with care.

Linearity and THD Factor

For large signal operation a nonlinear transfer function occurs, that means we have more gain on one half cycle of the output signal than on the other half. This is called amplitude distortion in the time domain, harmonic distortion in the frequency domain or nonlinear distortion when one is interested in the cause of the distortion. All these names are synonyms for the kind of distortion that occurs with a sine wave input.
Linearity of the amplifier is an important requirement that can be measured by the total harmonic distortion (THD). This is the rms value of the harmonic components of the output signal, excluding the fundamental, expressed as a percentage of the rms of the fundamental. For a nonlinear amplifier with a harmonic input the output can be expressed as a Fourier series as follows:

$$v_i = \hat{V}_i \cos\omega t$$

$$v_o = V_{o0} + \hat{V}_{o1}\cos(\omega t + \varphi_1) + \hat{V}_{o2}\cos(2\omega t + \varphi_2) + \hat{V}_{o3}\cos(3\omega t + \varphi_3) + \ldots$$

The percent second harmonic distortion factor is: $HD_2 = \frac{V_{o2}}{V_{o1}} 100\,\%.$

The total harmonic distortion factor can be computed with one of the formulas:

$$THD = \frac{\sqrt{V_{o2}^2 + V_{o3}^2 + \ldots}}{V_{o1}} 100\,\%, \qquad \text{or} \qquad THD = \sqrt{HD_2^2 + HD_3^2 + \ldots}\,\%.$$

Efficiency

The output stage must deliver the required amount of power in an efficient manner. This implies that the power dissipated in the output stage transistor(s) must be as low as possible. The power dissipated in a transistor raises its internal temperature and there is a maximum temperature (in the range of 150 to 200 degrees Celsius for silicon devices) above which the transistor is destroyed.
Efficiency of an amplifier is the ratio of the *ac* output power to the *dc* supply power:

$$\eta = \frac{P_o}{P_{DC}}.$$

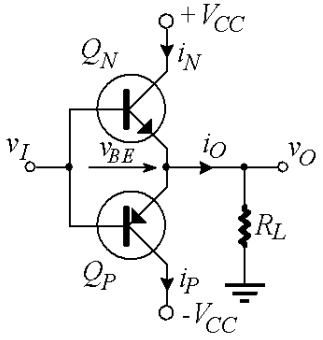
Classification of Output Stags

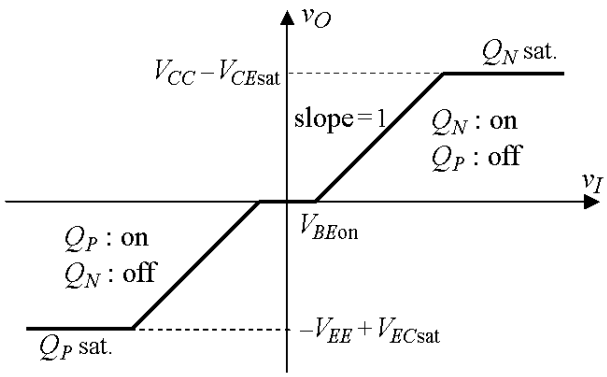
The output stages are classified according to the collector current waveform that results when an input signal is applied.
The class A stage is biased at a current greater than the amplitude of the signal current $I_C > I_{c\_pk}$ and the transistor conducts for the entire cycle of the input signal, that is, the conduction angle is 360°.

A transistor in a class B stage is biased at zero dc current and conducts for only half of the cycle of the input sine wave, resulting in a conduction angle of $180°$. The negative halves of the sinusoid will be supplied by other transistor (that also operates in class B mode) and conducts during the alternate half cycles.
An intermediate class between A and B, named class AB, involves biasing the transistor at a non-zero dc current, much smaller than the peak current of the sine wave. The conduction angle is slightly greater than $180°$ (but much less than $360°$).
In a class C amplifier, the transistor conducts for an interval shorter than that of a half-cycle and thus the conduction angle is much less than $180°$. The result is a periodically pulsating current waveform. To obtain a sinusoidal output voltage, this current is passed through an LC circuit, tuned to the frequency of the input sinusoid that acts as a low-pass filter and provides an output voltage that is proportional to the fundamental component in the Fourier series representation of the current.
Class A, B and AB amplifiers are employed as output stages of op amp and audio power amplifiers. Class C amplifiers are usually employed for radio frequency power amplifiers.

Class B Output Stage

The circuit consists of a complementary pair of transistors (that is a *npn* and a *pnp*) connected as emitter-followers. The transistors conduct on opposite alternations of the input cycle.





Circuit Operation

When the input voltage v_I is zero, both transistors are cutoff, the current i_O is zero and the output voltage v_O is zero.
As v_I goes positive (for the positive half cycle of the input) and exceeds the base-emitter voltage threshold, $V_{BE\text{on}} \approx 0.6\text{V}$, Q_N conducts; it supplies the load current $i_O = i_N$ and operates as an emitter follower: $v_O = v_I - v_{BE} = v_I - V_D$ ($v_{BE} \approx V_D$).
The E-B junction of Q_P is reversed biased (by $v_{EB} = -v_{BE} < 0$) and Q_P will be cutoff.
As the input goes negative by more than about 0.6V, Q_P turns on and it acts as an emitter follower: $v_O = v_I + v_{EB} = v_i + V_D$ ($v_{EB} \approx V_D$). In this case Q_P sinks current from load: $i_P = -i_O$ and Q_N will be cutoff.
The circuit operation is in a push-pull fashion: Q_N pushes (sources) current into the load when v_I is positive and Q_N pulls (sinks) current from the load when v_I is negative.
There exists a range of v_I centered around zero where both transistors are cutoff and v_O is zero. The dead band results in the “crossover distortion”. The effect of the crossover distortion will be more pronounced when the amplitude of the input signal is small.

Power Conversion Efficiency

To calculate the power conversion efficiency, η, of the class B stage, we neglect the crossover distortion and consider the case of output voltage peak amplitude:

$\hat{V}_o = k_v \cdot V_{CC}$, with $k_v = 0 \ldots 1$ being the power supply utilizing coefficient.

The average load power will be: $P_o = \frac{1}{2}\frac{\hat{V}_o^2}{R_L} = \frac{1}{2}\frac{k_v^2 \cdot V_{CC}^2}{R_L}$.

The current drawn from each supply will consist of half sine wave with a peak: $\hat{I}_o = \frac{\hat{V}_o}{R_L}$.

The average current and the average power drawn from each of the two power supplies will be the same:

$$I_C = \frac{1}{2\pi}\int_0^{\pi}\left(\hat{I}_c \sin \omega t\right) d\omega t = \frac{\hat{I}_c}{\pi} = \frac{\hat{I}_o}{\pi} = \frac{k_v \cdot V_{CC}}{\pi \cdot R_L},\ P_{DC} = 2I_C \cdot V_{CC} = \frac{2k_v}{\pi}\frac{V_{CC}^2}{R_L}.$$

The efficiency is: $\eta = \frac{P_o}{P_{DC}} = \frac{1}{2}\frac{k_v^2 \cdot V_{CC}^2}{R_L} \cdot \frac{\pi \cdot R_L}{2k_v V_{CC}^2} = \frac{\pi}{4} k_v$.

The maximum efficiency is obtained when v_O is at its maximum. This maximum value is limited by the transistors saturation to $V_{CC} - V_{CE\text{sat}}$ (almost V_{CC}). At this value (of the output voltage peak) $k_v \approx 1$ and the maximum (theoretical) power efficiency is: $\eta_{\max} \cong \frac{\pi}{4} = 78.5\,\%$.

This value is much larger than that obtained in the class A stage (25%). The maximum average power available from a class B output stage is: $P_{o\max} = \frac{1}{2}\frac{V_{CC}^2}{R_L}$ (for $k_v = 1$, that is a theoretical value).

Power Dissipation

The quiescent power dissipation of the class B stage is zero. When an input signal is applied, the average power dissipated is:

$$P_d = P_{DC} - P_o = P_{DC} - \eta P_{DC} = P_{DC}(1-\eta) = \frac{2k_v}{\pi}\frac{V_{CC}^2}{R_L}\left(1 - \frac{\pi}{4}k_v\right).$$

Since P_D depends on k_v by a parabolic (2nd order) function, we must find the worst case power dissipation, $P_{D\max}$. Differentiating equation with respect to k_v and equating to zero gives the value of k_v (named k_{vd}) that results in a maximum average power dissipation as:

$$\frac{\partial P_d}{\partial k_v} = 1 - \frac{\pi}{2}k_{vd} = 0,\ \ k_{vd} = \frac{2}{\pi} = 0.64.$$

At this point of maximum power dissipation, the efficiency can be evaluated:

$\eta = \frac{\pi}{4}\frac{2}{\pi} = \frac{1}{2} = 50\,\%$. That means the output power is equal to the dissipated power:

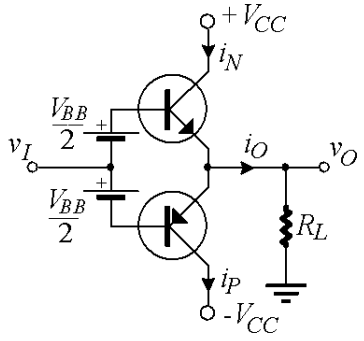
$P_{D\max} = P_o(k_{vd}) = \frac{1}{2}\frac{k_{vd}^2 \cdot V_{CC}^2}{R_L} = k_{vd}^2 P_{o\max}$ ($P_{o\max} = \frac{1}{2}\frac{\hat{V}_o^2}{R_L}$ being the maximum output power).

The maximum dissipated power is: $P_{D\max} = k_{vd}^2 P_{o\max} = \frac{4}{\pi^2} P_{o\max}$.

The power rating of each transistor must be greater than one fifth of the maximum possible output power: $P_{D1\max} = \frac{P_{D\max}}{2} = \frac{2}{\pi^2} P_{o\max} \cong 0.2 \cdot P_{o\max}$.

Class AB Output Stage

Crossover distortion can be virtually eliminated by biasing the output transistors at a small non-zero current. The result is a class AB output stage. A bias voltage V_{BB} is applied between the bases of Q_N and Q_P. For v_I=0, v_O=0 and a voltage $V_{BB}/2$ appears across the B-E junctions of Q_N and Q_P.



Assuming matched devices, the currents are:

$$i_N = i_P = I_Q = I_S \exp\frac{V_{BB}}{2 \cdot V_T}.$$

The value of V_{BB} is selected so as to yields the required quiescent current I_Q.

Circuit Operation

When v_I goes positive by a certain amount, the voltage at the base of Q_N increases by the same amount and the output becomes positive at an almost equal value:

$$v_O = v_I + \frac{V_{BB}}{2} - v_{BEN}.$$

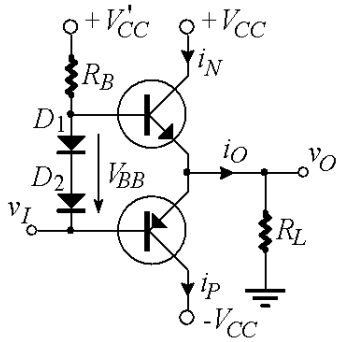
The positive v_O causes a current i_O to flow through R_L and the current: $i_N = i_P + i_O$ must increase and v_{BEN} increases slightly above $V_{BB}/2$. Because V_{BB} remains constant v_{EBP} decreases (with the same value that v_{BEN} increases) and i_P decreases to zero. With the exponential model of transistors we get:

$$v_{BEN} + v_{EBP} = V_{BB}, \quad V_T \ln\left(\frac{i_N}{I_S}\right) + V_T \ln\left(\frac{i_P}{I_S}\right) = 2 \cdot V_T \ln\left(\frac{I_Q}{I_S}\right) \qquad \text{that gives: } i_N \cdot i_P = I_Q^2.$$

Thus as i_N increases, i_P decreases by the same ratio (while the product remains constant). Class AB stage operates in much the same manner as the class B circuit, with one important exception: for small v_I, both transistors conducts and as v_I is increased or decreased, one of the two transistors takes over the operation.

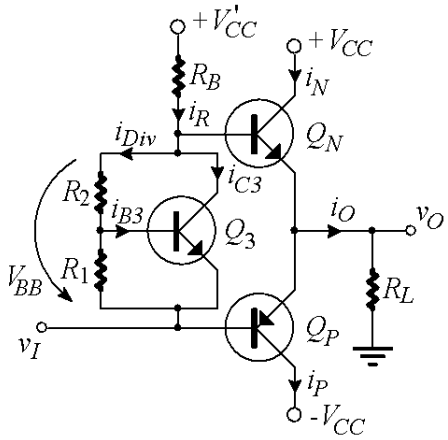
Biasing the Class AB Circuit

A current to voltage converter is used to provide the bias voltage between the transistor bases; the usual implementations are with diodes or with the V_{BE} multiplier circuit.



1. **Biasing circuit with diodes** gives a bias voltage:
$V_{BB} = v_{BEN} + v_{EBP} = v_{D1} + v_{D2} \cong 2 \cdot V_D$.
The current in diodes flows through the resistor R_B. The diode bias arrangement provides thermal stabilization of the quiescent current in the output stage. If the diodes are in close thermal

contact with the output transistors, theirs temperature will increase by the same amount as that of Q_N and Q_P. Thus V_{BB} will decrease at the same rate as $v_{BEN}+v_{EBP}$ with the result that I_Q remains almost constant (a diode and a B-E junction thermal coefficients are similar: $k_T=-2\,\mathrm{mV/°C}$).



2. **The V_{BE} multiplier bias circuit** with Q_3, R_1 and R_2 provides the designer with more flexibility. If we neglect the base current of the bias transistor Q_3:

$$I_{R_1}=\frac{V_{BE3}}{R_1}=I_{Div}-I_{B3}\cong I_{Div}\ (\text{for } I_{B3}<<I_{Div}).$$

The voltage V_{BB} across the bias network will be:

$$V_{BB}=I_{Div}(R_1+R_2)=V_{BE3}\left(1+\frac{R_2}{R_1}\right).$$

Thus the circuit simply multiply multiplies V_{BE3} by the factor $(1+R_2/R_1)$, and is known as "V_{BE} multiplier". The multiplication factor is under the designer's control and can be used to establish the value of V_{BB} required to yield a desired current I_Q.

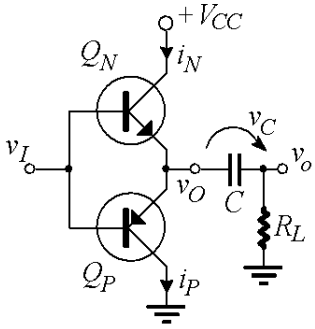
For positive v_i, especially near its peak value, the base current of Q_3 becomes sizable and reduces the current available for the V_{BE}-multiplier. Since large changes in i_{c3} correspond to only small changes in v_{BE3}, the decrease in current will be mostly absorbed by Q_3, leaving I_{Div}, and hence V_{BB}, almost constant.

The V_{BE}-multiplier circuit provides thermal stabilization of I_Q if Q_3 is in close thermal contact with the output transistors.

Single-Supply Operation

The class B (and AB) stage can be operated from a single supply, in which case the load is capacitively coupled through C.

For all frequencies of the input signal, the capacitor reactance should be negligible: $X_C<<R_L$.



For an input voltage (provided by the previous stage):

$$v_I=\frac{V_{CC}}{2}+V_{BE}+v_i\text{, we get } v_O=\frac{V_{CC}}{2}+v_o.$$

Without signal: $v_i=0\Rightarrow v_o=0$, $v_O=\frac{V_{CC}}{2}$ and $v_C=v_O-v_o=\frac{V_{CC}}{2}$.

For the positive half cycle of the signal, $v_i>0$, Q_N is ON and the current path (for i_N) is from V_{CC} through Q_N, C, R_L to ground. The capacitor C is slightly charged (because the conduction time, $T/2$, is much less than the circuit time constant, R_LC).

For the negative half-cycle of the signal, $v_i<0$, Q_P is ON and the current path (for i_P) is from the ground through C, Q_P, to ground. The capacitor acts as a power suurce and it is slightly discharged (with the same amount of charge that charges it in the positive half-cycle).

Power BJTs

Power transistors dissipate large amount of power in their collector-base junction. The dissipated power is converted into heat, which raises the junction temperature and there is a maximum temperature, $T_{J\max}$, above which the transistor could suffer permanent damage. For silicon devices $T_{J\max}$ is in the range from $150°C$ to $200°C$ (specified in the transistor data-sheet).

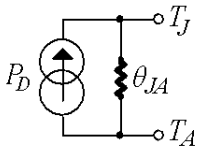
Thermal Resistances

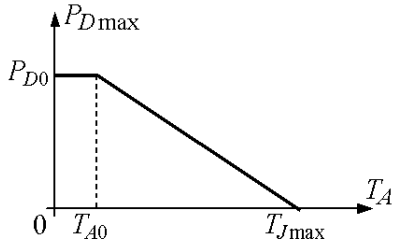
For a transistor operating in free air which is dissipating P_D watts, the temperature of the junction, relative to the surrounding ambience, can be expressed as:

$$T_J - T_A = \theta_{JA} \cdot P_D$$

where θ_{JA} is the thermal resistance between junction and ambiance, having units of °C per watt. θ_{JA} is usually specified on the transistor data-sheet.

The equation that describes the thermal-conduction process is analogue to Ohm's law, which describes the electrical conduction process. In this analogy, power dissipation corresponds to electrical current, temperature difference corresponds to voltage difference and thermal resistance corresponds to electrical resistance. Thus, we may represent the thermal-conduction process by an electric circuit.





On the right graph there is represented the maximum allowable power versus ambient temperature for a transistor in free air (based on the previous equation).

Power Dissipation versus Temperature

The maximum power dissipation is specified on the transistor data-sheet for an ambient temperature bellow T_{A0} (usually $25°C$). If the device is to be operated at higher ambient temperature, the maximum allowable power dissipation must be derated (according to the straight line in the previous figure). From the previous equation, one can compute:

$$\theta_{JA} = \frac{T_{J\max} - T_{A0}}{P_{D0}} \quad \text{or} \quad P_{D\max} = \frac{T_{J\max} - T_A}{\theta_{JA}}.$$

Heat Sink

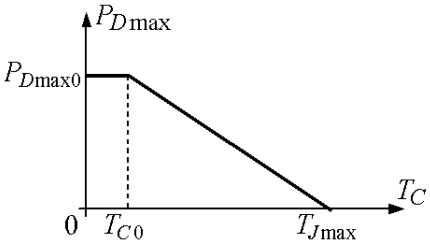
The heat sink is a piece of metal which the transistor is in thermal contact with. For a transistor with heat sink, the thermal resistance between junction and ambient consists on the thermal resistance between junction and transistor case plus the thermal resistance between case and ambiance:

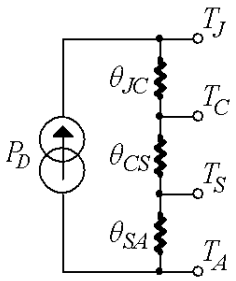
For a given transistor θ_{JC} is fixed by the device design and packaging. The designer can reduce θ_{CA} below its free air value if a heatsink is utilized. In this case: $\theta_{CA} = \theta_{CS} + \theta_{SA}$.

The electrical analog of the thermal-conduction process when a heatsink is employed can be drawn using the formulae: $T_J - T_A = P_D \cdot (\theta_{JC} + \theta_{CS} + \theta_{SA})$.

The device manufacturer usually supplies a derating curve for $P_{D\max}$ versus the case temperature:

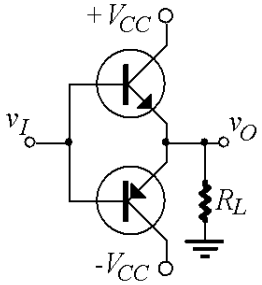
$$P_{D\max} = \frac{T_{J\max} - T_C}{\theta_{JC}}$$





The $P_{D\max}$ level of power dissipation cannot be achieved in practice; it would require an infinite sink and $T_A \leq 25°\text{C}$). Normally $P_{D\max}$ watts transistors can dissipate about $0.4P_{D\max}$ for a reasonable heatsink.

Applications



S9 – P1. For the class B output stage in figure let $V_{CC} = 6\,\text{V}$ and $R_L = 4\,\Omega$. If the output is a sinusoid with $4.5\,\text{V}$ peak determine:

a) The output power;
b) The average power drawn from each supply.
c) The power efficiency obtained at the given output voltage.
d) The peak currents supplied by v_I assuming that $\beta_N = \beta_P = 50$.
e) The maximum power that each transistor must be capable of dissipating safely.

a) $P_o = \frac{1}{2}\frac{\hat{V}_o^2}{R_L} = \frac{4.5^2}{2 \cdot 4} = 2.53\,\text{W};$

b) $I_C = \frac{\hat{I}_o}{\pi} = \frac{\hat{V}_o}{\pi \cdot R_L} = \frac{4.5}{\pi \cdot 4} = 0.358\,\text{A}, \qquad P_{DC+} = P_{DC-} = I_C \cdot V_{CC} = 0.36 \cdot 6 = 2.15\,\text{W};$

c) $\eta = \frac{P_o}{P_{DC}} = \frac{P_o}{P_{DC+} + P_{DC-}} = \frac{2.53}{2 \cdot 2.15} = 0.59 = 59\,\%;$

d) $i_I = \frac{i_o}{\beta + 1}, \qquad i_{I\_\max} = \frac{\hat{I}_o}{\beta + 1} = \frac{\hat{V}_o}{(\beta + 1) \cdot R_L} = \frac{1}{51} \cdot \frac{4.5}{4} = \frac{1.125}{51} = 22\,\text{mA};$

e) $P_{D\max 1} = \frac{P_{D\max}}{2} = \frac{2}{\pi^2} P_{o\max} \cong 0.2 P_{o\max} = 0.2 \frac{V_{CC}^2}{2R_L} = 0.2 \frac{6^2}{2 \cdot 4} = 0.2 \cdot 4.5 = 0.9\,\text{W}.$

S9 – P2. It is required to design a class B output stage to deliver an output power of $20\,\text{W}$ to an $8\,\Omega$ load. The power supply is selected such that V_{CC} is about 5 V greater than the peak output voltage. Determine the supply voltage required, the peak current drawn from each supply, the total power supply and the power conversion efficiency. Also determine the maximum power that each transistor must be able to dissipate safely.

Since $P_o = \frac{\hat{V}_o^2}{2R_L}$, then $\hat{V}_o = \sqrt{2P_oR_L} = \sqrt{2 \cdot 20 \cdot 8} = 17.9\,\text{V};$ We select : $V_{CC} = \hat{V}_o + 5 \cong 23\,\text{V}.$

The peak current drawn from each supply is: $\hat{I}_o = \dfrac{\hat{V}_o}{R_L} = \dfrac{17.9}{8} = 2.24\,\text{A}.$

The average power drawn from each supply is:

$P_{DC+} = P_{DC-} = \dfrac{\hat{I}_o}{\pi} \cdot V_{CC} = \dfrac{2.36}{\pi} 24 \cdot 23 = 16.4\,\text{W};$ and $P_{DC} = P_{DC+} + P_{DC-} = 2 \cdot 16.4 = 32.8\,\text{W};$

The power conversion efficiency is: $\eta = \dfrac{P_o}{P_{DC}} = \dfrac{20}{32.8} = 0.61 = 61\%;$

The maximum power dissipated in each transistor is: $P_{D\max 1} = \dfrac{2}{\pi^2} \dfrac{V_{CC}^2}{2R_L} = \dfrac{2 \cdot 23^2}{\pi^2 \cdot 2 \cdot 8} = 6.7\ \text{W}.$

S9 – P3. A BJT is specified to have maximum power dissipation P_{D0} of 2 watts at an ambient temperature T_A of $25\,^\circ\text{C}$ and a maximum junction temperature $T_{J\max}$ of $150\,^\circ\text{C}$. Find the following:

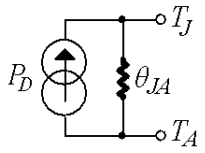
a) The thermal resistance θ_{JA};

b) The maximum power that can be safely dissipated at an ambient temperature of $50\,^\circ\text{C}$;

c) The junction temperature if the device is operated at $T_A = 25\,^\circ\text{C}$ and it is dissipating $1\ \text{W}$.

a) $\theta_{JA} = \dfrac{T_{J\max} - T_{A0}}{P_{D0}} = \dfrac{150 - 25}{2} = 62.5\,^\circ\text{C/W};$

b) $P_{D\max} = \dfrac{T_{J\max} - T_A}{\theta_{JA}} = \dfrac{150 - 50}{62.5} = 1.6\,\text{W};$



c) $T_J = T_A + \theta_{JA} P_D = 25 + 62.5 = 87.5\,^\circ\text{C}.$ $\quad (T_J - T_A = \theta_{JA} P_D)$

S9 – P4. A BJT is specified to have $T_{J\max} = 150\,^\circ\text{C}$ and to be capable of dissipating the following power: $P_{D\max 0} = 40\,\text{W}$ at $T_C = 25\,^\circ\text{C}$ and $P_{D0} = 2\,\text{W}$ at $T_A = 25\,^\circ\text{C}$. Find the following:

a) The thermal resistances θ_{JA} and θ_{JC};

b) The maximum power that can be dissipated safely by this transistor when it is operated in free air at $T_A = 50\,^\circ\text{C}$;

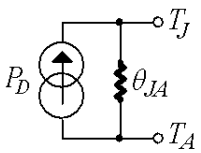
c) The maximum power that can be dissipated safely by this transistor when it is operated at an ambient temperature of $50\,^\circ\text{C}$, but with a heatsink for which $\theta_{CS} = 0.5\,^\circ\text{C/W}$ and $\theta_{SA} = 4\,^\circ\text{C/W}$. In this case find the temperature of the case and of the heatsink.

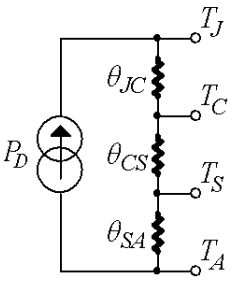
d) If the transistor is connected to a heatsink using an insulated washes for which the thermal resistance is and for an ambient temperature of $0.6\,^\circ\text{C/W}$, what heatsink thermal resistance is required to obtain safe operation at $10\,\text{W}$ power dissipated.

a) $\theta_{JA} = \dfrac{T_{J\max} - T_{A0}}{P_{D0}} = \dfrac{150 - 25}{2} = 62.5\,^\circ\text{C/W};$

$\theta_{JC} = \dfrac{T_{J\max} - T_{A0}}{P_{D\max 0}} = \dfrac{150 - 25}{40} = 3.12\,^\circ\text{C/W};$ (as with an infinite heatsink)

b) $P_{D\max} = \dfrac{T_{J\max} - T_A}{\theta_{JA}} = \dfrac{150 - 50}{62.5} = 1.6\ \text{W};$





c) $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} = 3.12 + 0.5 + 4 = 7.62\,^{\circ}\mathrm{C/W};$

$P_{D\max} = \dfrac{T_{J\max} - T_A}{\theta_{JA}} = \dfrac{150-50}{7.62} = 13.1\,\mathrm{W};\ T_S = T_A + \theta_{SA} P_D = 50 + 4 \cdot 13.1 = 102.4\,^{\circ}\mathrm{C};$

$T_C = 102 + 0.5 \cdot 13.1 = 109\,^{\circ}\mathrm{C};\ (T_J = 109 + 3.12 \cdot 13.1 = 150\,^{\circ}\mathrm{C}).$

d) $\theta_{JA} = \dfrac{T_{J\max} - T_A}{P_D} = \dfrac{150-40}{10} = 11^{\circ}\mathrm{C/W};\ \ \theta_{SA} = \theta_{JA} - \theta_{JC} - \theta_{CS} = 11 - 3.12 - 0.6 = 7.28\,^{\circ}\mathrm{C/W}.$