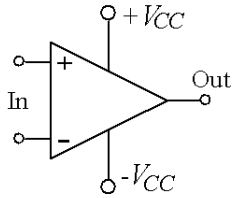
Operational Amplifiers

The operational amplifier (OpAmp) is a dc-coupled, high-gain voltage amplifier with a differential input and a single output (usually).
An important characteristic of the opamp is that they are direct-coupled devices or dc amplifiers – dc stands for direct-coupled or equally well stands for direct-current, since a dc amplifier is one that amplifies signals whose frequency is as low as zero.

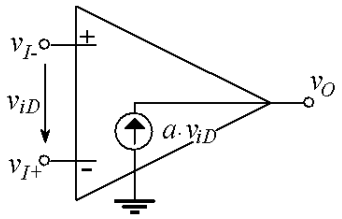
Symbol and Terminals

The two input terminals are called: the inverting input (–) and the non-inverting input (+). The typical OpAmp operates with two dc power supplies, one positive and one negative. Usually the power supply terminals are left off the schematic symbol for simplicity, but are always understood to be there.



The Ideal OpAmp

The ideal OpAmp has infinite voltage gain, infinite input resistance, zero output resistance and infinite bandwidth. The differential input voltage appears between the two input terminals: $v_{ID} = v_{I+} - v_{I-}$ and the output voltage is: $v_O = a \cdot v_{ID} = a \cdot (v_{I+} - v_{I-})$, where a is the differential gain.



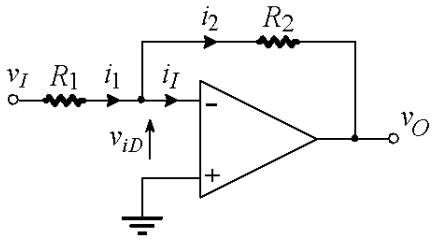
The OpAmp responds only to the difference signal and ignores any signal common to both inputs. We call this property common-mode rejection and we conclude that an ideal OpAmp has infinite common-mode rejection.

Saturation Voltages

The voltage at the OpAmp output is limited by saturation voltages: $-V_{sat-} \le v_O \le +V_{sat+}$.
Ideally, the magnitude of saturation voltages is: $V_{sat-} = V_{sat+} = V_{CC}$.
Practically, a first approximation for the saturation voltages is: $V_{sat-} = V_{sat+} = V_{CC} - 2$. (The saturation voltages are about 2 V below the power supply.)

The Inverting Configuration

The amplifier presented in figure has a gain: $A = \frac{v_O}{v_I}$.



An ideal opamp will be considered. As long as the output voltage is finite (output not saturated: $-V_{sat-} < v_O < +V_{sat+}$), the voltage between the opamp input terminals is zero (practically, negligibly small): $v_{ID} = \frac{v_O}{a} = \frac{v_O}{\infty} = 0$.

Since $v_{ID} = v_{I+} - v_{I-} = 0$, it follows that $v_{I+} = v_{I-}$; we speak of this as: the two input terminals are "tracking each other in potential". We also speak of a "virtual short circuit" that exists between the two input terminals (virtual short, not physically shorted).

Because $v_{I+}=0$ (the non-inverting terminal is grounded), it follows that $v_{I-}=0$; we speak of the inverting terminal as being a "virtual-ground" – that is having zero voltage, but not physically connected to ground.

The input current is: $i_1=\frac{v_I-v_{I-}}{R_1}=\frac{v_I}{R_1}$.

This current cannot flow into the opamp, since the ideal opamp has infinite input resistance and hence draw zero current ($i_I=0$):

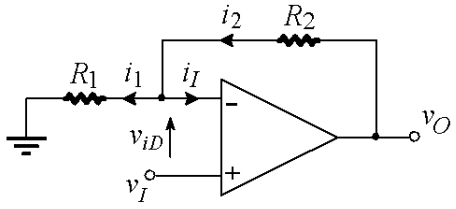
$i_1=i_I+i_2=i_2$,

$v_O=v_{I-}-i_2R_2=0-i_1R_2=-\frac{v_I}{R_1}R_2$, and the voltage gain is: $A_v=\frac{v_o}{v_I}=-\frac{R_2}{R_1}$.

Because of the minus sign this configuration is called the inverting configuration.
The resulted voltage gain is much smaller than a but is stable and predictable. That is, we trade gain for accuracy.

The input resistance of the amplifier is: $R_i=\frac{v_I}{i_I}=\frac{v_I}{i_1}=\frac{v_I}{v_I/R_1}=R_1$.

The Non-Inverting Configuration



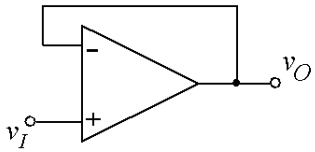
The circuit is presented in figure; the input and the ground terminal from the inverting configuration are interchanged.
The virtual short-circuit between the opamp input terminals gives: $v_{I-}=v_{I+}=v_I$.

The input current is zero because of the infinite input resistance and: $i_2=i_I+i_1=i_1$,

$i_1=\frac{v_{I-}}{R_1}=\frac{v_I}{R_1}$, $v_O=R_2i_2+v_{I-}=R_2i_1+v_I=R_2\frac{v_I}{R_1}+v_I$, which yields a voltage gain:

$$A_v=\frac{v_o}{v_I}=1+\frac{R_2}{R_1}.$$

The gain is positive – hence the name of the non-inverting amplifier.
The input resistance of this amplifier is ideally infinite since no current will flow into the non-inverting terminal of the opamp.

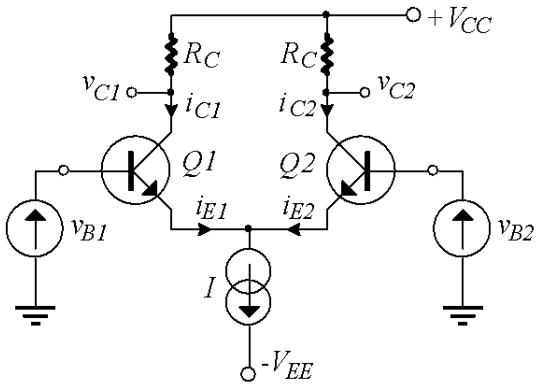


The circuit can be used as a buffer amplifier to connect a source with high impedance to a low-impedance load. In many applications the buffer is not required to provide any voltage gain; rather it is used mainly as an impedance transformer.
For $R_2=0$ and $R_1=\infty$ (without R_2) we obtain the simplest unity gain amplifier or voltage follower (the output voltage follows the input voltage: $A_v=1$ and $v_O=v_I$).

The Differential Amplifier

The differential amplifier is the most widely used circuit in analog integrated circuits. For instance, the input stage of op-amp is a differential amplifier.

The basic differential-pair configuration consists of two matched transistors Q_1 and Q_2, whose emitters are joined together and biased by a constant-current source I. The signal sources must provide *dc* paths for the base-bias currents. Consider first the case when the two bases are joined together and connected to a common-mode voltage v_{CM}: $v_{B1} = v_{B2} = v_{CM}$. Since the two transistors are matched, it follows from symmetry that the current I will divide equally between the two devices (the transistor current is given by the basic equation of the BJT; for each of the two transistors the current depends on the identical v_{BE} and the identical transistor parameters).



Since $i_C \approx i_E$, it follows that $i_{C1} = i_{C2} \approx I/2$. The emitter voltage is $v_E = v_{CM} - v_{BE}$, where v_{BE} is the voltage corresponding to the emitter current $i_E = I/2$.

The voltage at each collector is: $v_C = V_{CC} - R_C I/2$, and the difference in voltage between the two collectors will be zero: $v_{C1} = v_{C2}$ and $v_{C1C2} = v_O = v_{C1} - v_{C2} = 0$.

Now let us vary the value of the common-mode input signal, v_{CM}. As long as Q_1 and Q_2 remain in the active regime the current I still divide equally between the two transistors and the voltage at the collector will not change. Thus, the differential pair does not respond to (or rejects) the common-mode input signals.

The limits of the output voltage

Consider $v_{B2} = 0$ and $v_{B1} >> 0$ (let's say $v_{B1} = 0.5\ \text{V}$). Q_1 will be "on" and conducting all of the current I and Q_2 will be "off". For the Q_1 to be "on", $v_E = v_{B1} - V_{BE} = 0.5 - 0.7 = 0.2\ \text{V}$ and $v_{BE2} = v_{B2} - v_E = 0.2\ \text{V}$ which keeps Q_2 "off". $i_{C1} = I$, $i_{C2} = 0$, $v_{C1} = V_{CC} - R_C I$ and $v_{C2} = V_{CC}$.

Let us change $v_{B1} = -0.5\ \text{V}$. Q_1 will turn off and Q_2 will carry all the current I.

$v_E = v_{B2} - V_{BE} = -0.7\ \text{V}$ and $v_{BE1} = v_{B1} - v_E = -0.5 - (-0.7) = 0.2\ \text{V}$ which keeps Q_1 "off".

$i_{C2} = I$, $i_{C1} = 0$, $v_{C2} = V_{CC} - R_C I$ and $v_{C1} = V_{CC}$.

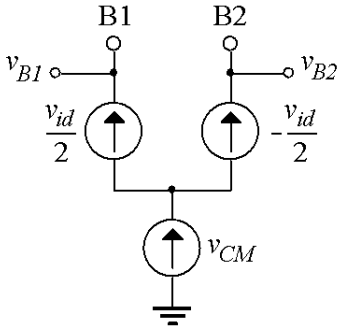
The maximum peak amplitude and peak-to-peak amplitudes of the output are:

$V_{Op} = V_{CC} - (-R_C I) = R_C I$ and $V_{Opp} = 2\ V_{Op} = 2 R_C I$.

From the above we see that the differential pair certainly responds to difference mode or differential signals. In fact, with relatively small difference voltages we can steer the entire bias current from one side of the pair to the other. This property is used in logic circuits for the emitter-coupled logic, which is the fastest logic circuit family.

To use the differential pair as a linear amplifier we can apply a very small differential signal. In this case the output voltage taken between the two collectors (the differential output) is proportional to the differential input signal (small-signal operation).

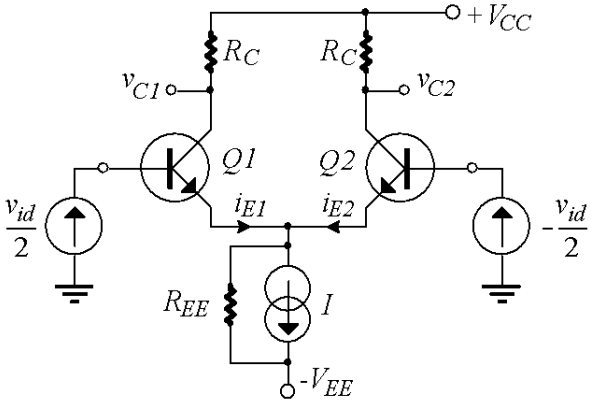
Small-Signal Operation



The input signal sources can be decomposed into a differential component and a common-mode component:
$v_{id} = v_{B1} - v_{B2}$ and $v_{CM} = (v_{B1} + v_{B2})/2$;
These are the difference and the average values of the signals take from the symmetrical points of the circuits, the inputs (base terminals) in this case.

The Differential Gain

Consider the differential amplifier fed by a purely differential signal, v_{id}, with $v_{CM} = 0$. It results: $v_{B1} = -v_{B2} = v_{id}/2$; the circuit for this case, represented in figure, includes also the output resistance of the current source, R_{EE}.

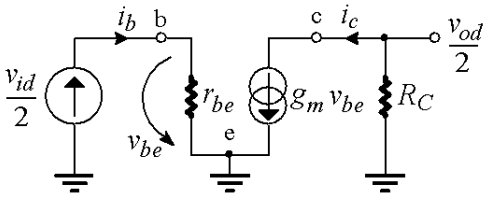


From the symmetry it follows that the signal voltage (*ac*) at the common emitter will be zero: $i_{c1} = i_{c2}$, $i_{e1} = i_{e2}$, $i_{ee} = i_{e1} + i_{e2} = 0$ and $v_e = R_{EE}\, i_{ee} = 0$.
The common emitter is connected to the ground from variation (signal) point of view. The circuit can be split in two identical parts and only one is needed to analyze the differential small-signal operation. The circuit that results is presented in figure and it is known as the "differential half-circuit".
The parameters of the amplifier can be computed as follows:

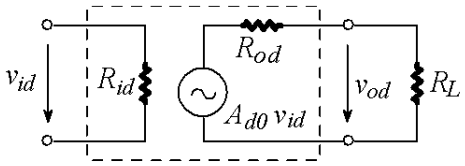
$$\frac{v_{od}}{2} = -g_m v_{be} R_C\,, \quad \frac{v_{id}}{2} = v_{be} \quad \text{and} \quad A_{d0} = \frac{v_{od}}{v_{id}} = -g_m R_C\,,$$

$$i_b = \frac{v_{id}}{2} \cdot \frac{1}{r_{be}}\,, \quad R_{id} = \frac{v_{id}}{i_b} = 2r_{be}\,;$$

$$i_o = \frac{v_{od}}{2R_C}\,, \quad R_{od} = \frac{v_{od}}{i_o} = 2R_C\,.$$



The equivalent differential amplifier in differential mode with load is presented in the next figure. The differential voltage gain with load can be computed as follows:



$$v_{od} = A_{d0} v_{id} \frac{R_L}{R_L + R_{od}} \quad \text{and}$$

$$A_d = \frac{v_{od}}{v_{id}} = A_{d0} \frac{R_L}{R_L + R_{od}} = -g_m R_C \frac{R_L}{R_L + 2R_C} = -g_m \left(R_C \parallel \frac{R_L}{2} \right).$$

Common-Mode Gain

We will consider a differential amplifier fed by a purely common-mode voltage signal v_{CM}:
$v_{CM} = v_{B1} = v_{B2}$; $v_{id} = v_{B1} - v_{B2} = 0$, the differential component of the input is zero.
From symmetry it follows that: $i_{c1} = i_{c2}$, $i_{e1} = i_{e2} (= i_e)$ and $i_{ee} = 2\, i_e$.

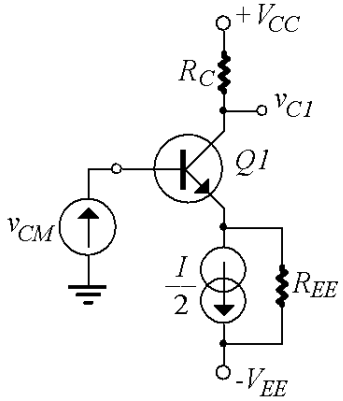
It follows that: $v_e = i_{ee} R_{EE} = 2\, i_e R_{EE}$. If we replace R_{EE} with two resistance of value $2R_{EE}$ in parallel (each of them on one transistor emitter) we can consider two independent circuits, so called common-mode half-circuits. The transistor in this circuit is biased by a current $I/2$ and has a resistance $2R_{EE}$ in the emitter lead, as it is indicated in figure.

The common-mode output is:

$$v_{c1} = -v_{CM} \frac{R_C}{2R_{EE} + r_e} \cong -v_{CM} \frac{R_C}{2R_{EE}}, \text{ since } R_{EE} >> r_e.$$

$v_{c2} = v_{c1} \cong -v_{CM} \dfrac{R_C}{2R_{EE}}$, the differential output is: $v_{od} = v_{C1} - v_{C2} = 0$.

If the output is taken single-ended (from a collector to ground), the common-mode gain is finite: $A_{cm} = \dfrac{v_{c1}}{v_{CM}} \cong -\dfrac{R_C}{2R_{EE}}$.



The Common-Mode Rejection Ratio

The differential gain for a single ended output is half of the pure differential gain:

$$A_{d0} = \frac{v_{c1}}{v_{id}} = -\frac{1}{2} g_m R_C.$$

The common-mode rejection ratio ($CMRR$) for a single-ended output is:

$$CMRR = \left| \frac{A_{d0}}{A_{cm}} \right| = \frac{1}{2} g_m R_C \frac{2R_{EE}}{R_C} = g_m R_{EE}.$$

The effect of the variations: of components parameters, produced by temperature and aging, of power supply voltages and so on, is identical for the two transistors in the differential amplifier and can be considered to be common-mode variations. As the circuit rejects common-mode signals, it is relatively insensitive to the variations considered earlier. It is the input differential stage in the op-amp circuit that primarily determines the op-amp characteristics (parameters). In monolithic integrated circuits (IC) the differential amplifiers are symmetrical because the integrated components are realized on the same chip and have virtually identical characteristics and hence a very high $CMRR$.

Current Sources

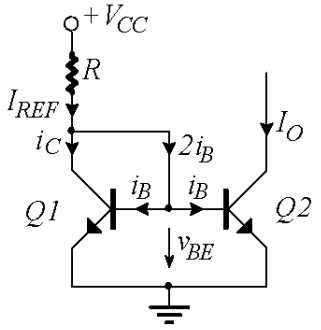
Biasing in ICs is based on the use of constant-current sources, such is the one used by the differential pair.

The Current Mirror

The current mirror consists of two matched transistors Q_1 and Q_2 which have the same v_{BE}, (with $B_1 \equiv B_2$ and $E_1 \equiv E_2$). Q_1 is connected as a diode, $C_1 \equiv B_1$.

The current mirror is fed by an input (reference) current I_{REF}, produced in the circuit of figure by the bias source V_{CC} and the resistor R: $I_{REF} = \dfrac{V_{CC} - V_{BE}}{R}$.

The output current can be computed based of the input current:



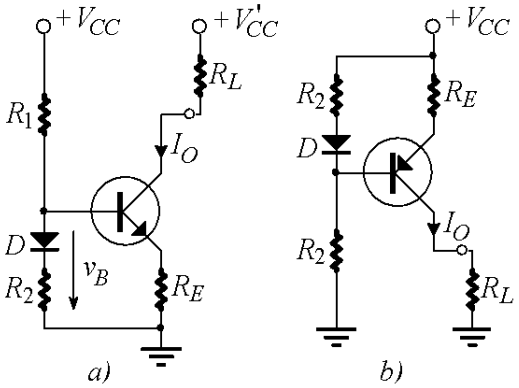
$I_{REF} = I_{C1} + I_{B1} + I_{B2} = \beta \cdot I_B + 2I_B = I_B(\beta + 2)$, $I_B = \dfrac{I_{REF}}{\beta + 2}$;

$I_O = \beta \cdot I_B = \dfrac{\beta}{\beta + 2} I_{REF}$. For $\beta >> 2$ the circuit acts as a current mirror: $I_O \cong I_{REF}$.

The circuit operates as a current source long as Q_2 remains in the active mode, practically for: $v_O > V_{CEsat} \cong 0.2 \ldots 0.3$ V.

The output resistance of the current source is: $R_o = r_o|_{Q_2} = \dfrac{V_A}{I_O}$.

The Standard Discrete Current Source



A current source generate a current that can be: either sink through the load (from a voltage supply) – that is the circuit with a *npn* transistor, figure *a)*, or source the current through a load (to the ground or to a negative terminal of a voltage supply) – that is the circuit with a *pnp* transistor as the one in fig. *b)*. For both circuits the diode D compensates the B-E junction voltage variations with temperature, theirs thermal coefficients being almost identical.
We compute the currents for circuit in figure *a)*:

$V_B = V_D + R_2 I_2 = V_{BE} + R_E I_E$, $V_D \cong V_{BE}$, $R_2 I_2 = R_E I_E$ and $I_E = \dfrac{R_2 I_2}{R_E}$.

For $I_1 >> I_B$, $I_1 = I_B + I_2 \cong I_2$ and $I_1 = \dfrac{V_{CC} - V_D}{R_1 + R_2} \cong I_2$.

The output current is: $I_O = I_C \cong I_E = \dfrac{R_2}{R_E} I_1 = \dfrac{R_2}{R_1 + R_2} \dfrac{V_{CC} - V_D}{R_E}$.

The Output Resistance

The output resistance of the current source, R_o, can be computed with the small-signal equivalent circuit, because the variations in current and hence in v_{BE} are very small.

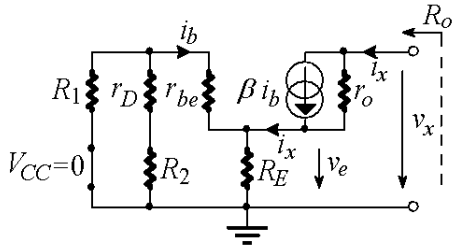
$r = R_1 \parallel (R_2 + r_D) + r_{be}$

$v_e = i_x \cdot (r \parallel R_E)$, $i_b = -\dfrac{v_e}{r} = -i_x \dfrac{R_E}{R_E + r}$

$v_x = v_e + (i_x - \beta \cdot i_b) \cdot r_o$,

$v_x = i_x (r \parallel R_E) + \left(1 + \beta \dfrac{R_E}{R_E + r}\right) \cdot i_x r_o$,

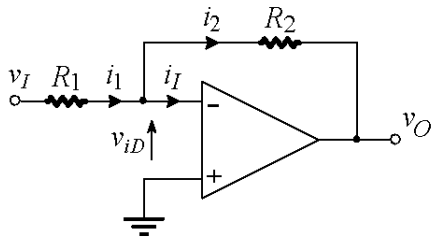
$R_o = \dfrac{v_x}{i_x} = (r \parallel R_E) + \left(1 + \beta \dfrac{R_E}{R_E + r}\right) \cdot r_o \cong r_o \left(1 + \beta \dfrac{R_E}{R_E + r}\right)$.



The output resistance of the circuit is much greater than the output resistance of the transistor, $R_o >> r_o$.

Applications

S10 – P1. Design an inverting amplifier having a gain of -100 with an input resistance of $10\ \text{k}\Omega$, using an ideal op-amp.



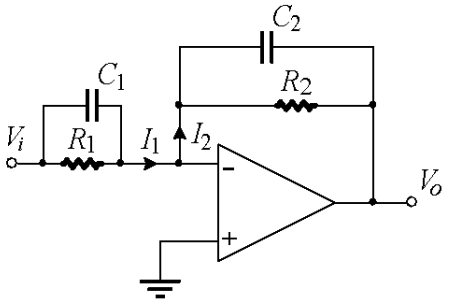
Ideal op-amp: $a=\infty$ will give: $v_{ID}=\dfrac{v_O}{a}=\dfrac{v_O}{\infty}=0$

and $R_i=\infty$ will give: $i_I=0$.

$$A_v=-\frac{R_2}{R_1}=-100,\quad R_2=100\,R_1;$$

$$R_i=\frac{v_I}{i_I}=R_1=10\,\text{k}\Omega \quad \text{and} \quad R_2=100\cdot 10\,\text{k}\Omega=1\,\text{M}\Omega.$$

S8 – P3. Find the transfer function of the circuit in figure assuming the op-amp to be ideal. Under what conditions is the transfer function a constant independent of frequency? For a gain of -10 and input impedance consisting on a $1\ \text{M}\Omega$ shunted by a $30\ \text{pF}$, what values of R_1, R_2, C_1 and C_2 must be used?



1. $I_1=V_i\cdot Y_1$, (with $Y_1=\dfrac{1}{R_1}+sC_1$); $I_2=-V_o\cdot Y_2$ (with $Y_2=\dfrac{1}{R_2}+sC_2$); $I_1=I_2$ gives:

$$V_i\cdot Y_1=-V_oY_2 \text{ and } V_o=-\frac{Y_1}{Y_2}V_i=-\frac{1/R_1+sC_1}{1/R_2+sC_2}V_i=-\frac{R_2}{R_1}\cdot\frac{1+sR_1C_1}{1+sR_2C_2}V_i.$$

(For sine wave the operator s is replaced by $j\omega$ and: $\underline{V_o}=-\dfrac{R_2}{R_1}\cdot\dfrac{1+j\omega R_1C_1}{1+j\omega R_2C_2}\underline{V_i}$.)

For the transfer function to be frequency independent it must be real (without s);

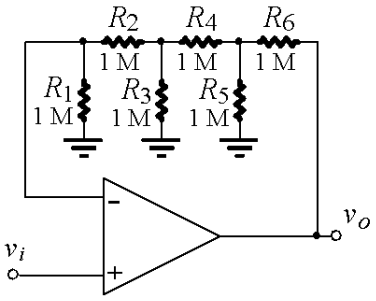
Because R_1, R_2, C_1 and C_2 are not zero, we must have: $1+sR_1C_1=1+sR_2C_2$;

That gives the frequency independence condition of the transfer function: $R_1C_1=R_2C_2$.

2. The input impedance is: $Y_i=Y_1$; as a result: $R_1=R_i=1\ \text{M}\Omega$, $C_1=C_i=30\ \text{pF}$;

The voltage gain gives the resistors ratio: $A_v=-\dfrac{R_2}{R_1}=-10\Rightarrow R_2=10\cdot R_1=10\ \text{M}\Omega$, and from the frequency independence condition we get: $C_2=\dfrac{R_1}{R_2}C_1=\dfrac{C_2}{10}=3\ \text{pF}.$

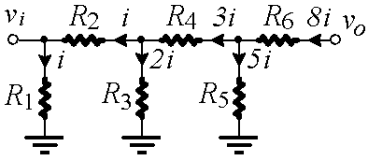
S8 – P3. Find the gain v_O/v_I of the amplifier circuit of figure assuming that the op-amp is ideal. *Hint*: Start at the left-hand side of the feedback circuit and work your way towards the output figuring out the various node voltages and branch currents in the feedback circuit.



Ideal op-amp: $a=\infty$ => $v_{ID}=\dfrac{v_O}{a}=0$ and $R_i=\infty$ => $i_I=0$.

The resistance network is presented in the next figure.

$v_{R1}=v_{I-}=v_I-v_{ID}=v_I$ and $i_{R2}=i_{R1}+i_I=i_{R1}=i$ (i is a simplified notation).



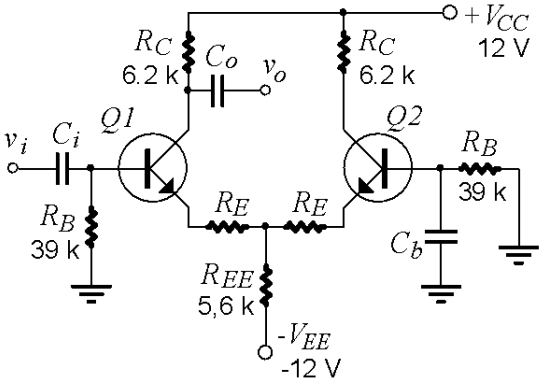
$$i_{R3}=\frac{v_{R3}}{R}=\frac{2Ri}{R}=2i\,;\qquad i_{R4}=i_{R1}+i_{R2}=i+2i=3i$$

$$i_{R5}=\frac{v_{R3}+v_{R3}}{R}=\frac{3Ri+2Ri}{R}=5i\,;\qquad i_{R6}=i_{R4}+i_{R5}=3i+5i=8i$$

$$v_O=v_{R6}+v_{R5}=8Ri+5Ri=13Ri\,(=13v)_I\,;$$

$$A_v=\frac{v_o}{v_I}=\frac{13Ri}{Ri}=13$$

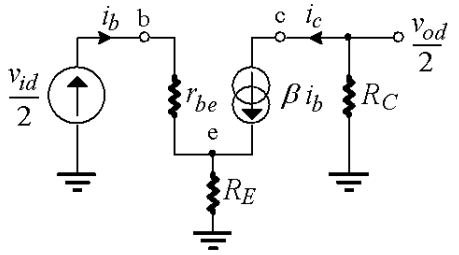
S9 – P1. *1)*. Find the voltage gain v_O/v_I and the input resistance of the amplifier in figure. Assume that Q_1 and Q_2 are identical transistors with: $\beta_1=\beta_2=\beta=200$ and $V_{BE1}=V_{BE2}=V_{BE}=0.6$ V.
Consider: *a)* $R_E=0$ and *b)* $R_E=100\,\Omega$.
2). How does the voltage gain and input resistance get modified if β is doubled.



1). Q point:

$I_{EE}=\dfrac{V_{EE}-V_{BE}}{R_{EE}+\dfrac{R_B}{2\beta}+\dfrac{R_E}{2}}=\dfrac{12-0.6}{5.6k+\dfrac{39k}{2\cdot 200}+\dfrac{0...100}{2}}=2.001...1.983\,\text{mA}$. We consider a rounded value $I_{EE}=2\,\text{mA}$ for both cases (R_E doesn't modify significantly the Q point – because R_E is much lower than R_{EE}); the current is equally divided by the two transistors and $I_E=I_{EE}/2=1\,\text{mA}$.

The transistor parameters are: $g_m=I_E/V_T=40\,\text{mA/V}$ and $r_{be}=\beta/g_m=5\,\text{k}\Omega$.



The "differential half-circuit" circuit is presented in figure.

$\dfrac{v_{od}}{2}=-\beta\cdot i_b R_C$, $\dfrac{v_{id}}{2}=r_{be}i_b+R_E(\beta+1)\cdot i_b$ and

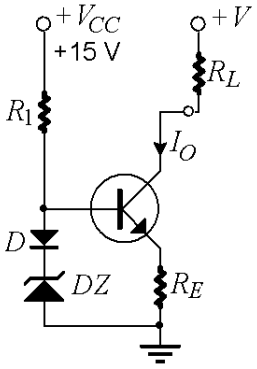
$$A_{d0}=\frac{v_{od}}{v_{id}}=-\frac{\beta\cdot R_C}{r_{be}+(\beta+1)\cdot R_E}\cong-\frac{R_C}{1/g_m+R_E}=-\frac{6.2k}{25+0...100}=-(248...50);$$

$$R_{id}=\frac{v_{id}}{i_b}\cong 2\cdot(r_{be}+\beta\cdot R_E)=2\cdot(5k+0...200\cdot 0.1k)=10...50\,\text{k}\Omega.$$

1). The differential voltage gain does not depend on β.

The differential input resistance would be doubled: $r_{be}=\beta/g_m=10\,\text{k}\Omega$ and $R_{id}\cong 2\cdot\left(r_{be}+\beta\cdot R_E\right)=2\cdot\left(10k+0...400\cdot 0.1k\right)=20...100\,\text{k}\Omega$.

S9 – P2. *a)* Design the current source in figure to operate at $I_Z=5\,\text{mA}$ and to provide a current $I_O=10\,\text{mA}$. The parameters of the DZ6V8 Zener diode are: $V_Z=6.8\,\text{V}$ and $r_Z=8\,\Omega$, the diode D has $V_D=0.7\,\text{V}$ and the transistor parameters are $\beta\geq 250$ and $V_{BE}=0.7\,\text{V}$.



b) What is the lowest voltage at the output; assume $V_{CEsat}=0.3\,\text{V}$.

c) Compute the output resistance of the current source R_o. Assume that $V_A=100\,\text{V}$ and $V_T=25\,\text{mV}$.

d) Calculate (estimate) the effect of R_L variation to the output current. (Consider $R_L=0\ldots 2\,\text{k}\Omega$ and $+V=30\,\text{V}$).

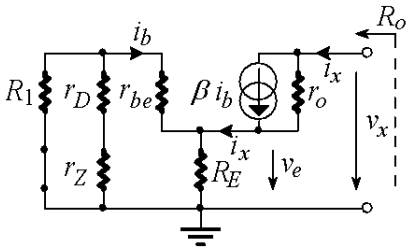
a) $I_C=I_O$ and $\beta\geq 250$ gives $I_B=\dfrac{I_C}{\beta}\leq\dfrac{10m}{250}=40\,\mu\text{A}$. $I_{R1}=I_Z+I_B$ and $5\,\text{mA}\leq I_{R1}\leq 5.04\,\text{mA}$.

$$R_1=\frac{V_{CC}-V_Z-V_D}{I_{R1}}=\frac{15-6.8-0.7}{5m}=1.5\,\text{k}\Omega.$$

$V_B=V_D+V_Z=V_{BE}+R_E I_E$ gives $I_O\cong I_E=\dfrac{V_D+V_Z-V_{BE}}{R_E}=\dfrac{V_Z}{R_E}$ and $R_E\cong\dfrac{V_Z}{I_O}=\dfrac{6.8}{10m}=680\,\Omega$.

b) $V_{CE}>V_{CEsat}$ gives the minimum output voltage: $V_{Cmin}=V_E+V_{CEsat}=V_Z+V_{CEsat}=7.1\,\text{V}$.

c) The current and v_{BE} variations are very small; the small-signal equivalent circuit gives:

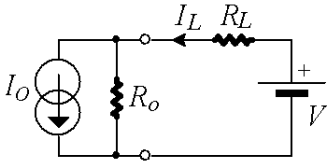


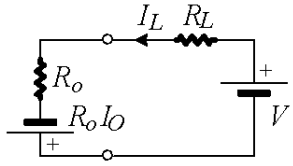
$$r_o=\frac{V_A}{I_C}=\frac{100}{10m}=10\,\text{k}\Omega,\ r_{be}=\frac{\beta}{40\cdot I_C}\geq\frac{250}{400m}=625\,\Omega.$$

$$r_D=\frac{V_T}{I_D}=\frac{25m}{5m}=5\,\Omega,\ r=R_1\parallel\left(r_Z+r_D\right)+r_{be}\cong r_{be}.$$

$$R_o=r_o\left(1+\beta\frac{R_E}{R_E+r}\right)\cong r_o\left(1+\frac{R_E}{R_E/\beta+1/g_m}\right)\geq 10k\left(1+\frac{680}{680/250+1/40\cdot 10m}\right)=1312\,\text{k}\Omega.$$

d) The current variations can be computed with the current generator equivalent circuit:





$$I_L=\frac{R_o I_O+V}{R_o+R_L},$$

$$\Delta I_L=\frac{R_o I_O+V}{R_o+R_{L2}}-\frac{R_o I_O+V}{R_o+R_{L1}}\cong\frac{\Delta R_L\left(R_o I_O+V\right)}{R_o^2}\cong\frac{R_o I_O}{R_o^2}\Delta R_L=\frac{I_O}{R_o}\Delta R_L\ \text{and}$$

$$\frac{\Delta I_L}{I_O}\cong\frac{\Delta R_L}{R_o}=\frac{2k}{1312k}=0.15\,\%.$$