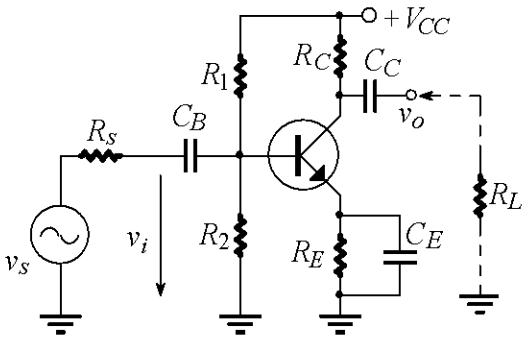
Classical Single Stage Transistor Amplifiers

The circuits will be analyzed with *ac-dc* superposition theorem.

The Common-Emitter Amplifier

The figure presents the circuit of the classical BJT amplifier in the common-emitter (CE) configuration. That means the emitter terminal is common to the input and to the output; the emitter is connected to ground from the signal point of view (through C_E).



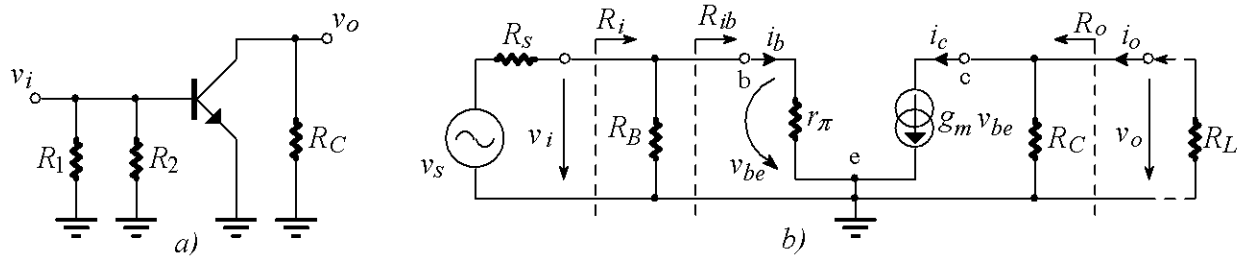
The signal source is coupled to the base of the transistor through coupling capacitor C_B and the output signal at the collector is coupled to the load, R_L, through another coupling capacitor C_C. The emitter capacitor C_E is called bypass capacitor; the signal current i_e will flow through C_E bypasing the emitter resistance R_E. These capacitors should be chosen sufficiently large so that they acts as short-circuits over the frequency range of interest (theirs reactace should be much lower than the resistances seen at theirs terminals).

DC Analysis

The capacitors are replaced with open-circuits; it results the voltage divider bias circuit that has been analised previously.

AC Analysis

The coupling and bypass capacitors are replaced by short-circuits; the *dc* power supply is also replaced by a short-circuit. The *ac* equivalent circuit that results is presented on the left side of the next figure. For small-signal ($v_{be} << V_T$) the transistor can be replaced by one of its small-signal model; on the right side of figure it is used the simplified hybrid-π model.



The open-circuit voltage gain

The voltage gain from base to collector, without load (computed with the small-signal equivalent circuit) is:

$$A_{v0} = \frac{v_o}{v_i} = \frac{-g_m v_{be} R_C}{v_{be}} = -g_m R_C$$

The minus sign in the formula indicates the phase inversion (of the output signal with respect to the input).

The Input Impedance

The input impedance looking in the transistor base and the total input impedance seen by the signal source are:

$$R_{ib} = \frac{v_{be}}{i_b} = r_\pi ; \qquad R_i = \frac{v_i}{i_i} = R_1 \parallel R_2 \parallel R_{ib} = R_B \parallel r_\pi .$$

The overall voltage gain, from source to output is given by the voltage divider at the input combined with the voltage gain:

$$A_v = \frac{v_o}{v_s} = \frac{v_o}{v_i}\frac{v_i}{v_s} = A_{v0}\frac{R_i}{R_i + R_s} = -g_m R_C \frac{R_i}{R_i + R_s} .$$

The output impedance

The output impedance is the Thevenin equivalent resistance at the output (looking from the load to the circuit with the independent source v_s suppressed):

$v_s = 0 \Rightarrow v_{be} = 0 \Rightarrow g_m v_{be} = 0$, the current source is an open-circuit and: $R_o = \left.\frac{v_o}{-i_o}\right|_{v_s=0} = R_C$.

Effect of Load on Voltage Gain

When a load R_L is connected to the output the collector resistance at the output is a parallel combination of the two resistances at the output and the equivalent *ac* collector resistance, R_c, will give the voltage gain:

$$A_v = \frac{v_o}{v_i} = -g_m R_c = -g_m \left(R_C \parallel R_L\right)$$

If one considers the voltage amplifier model, a voltage divider will be present at the output and the voltage gain (computed in a different manner) is the same:

$$A_v = A_{v0}\frac{R_L}{R_L + R_o} = -g_m R_C \frac{R_L}{R_L + R_o} = -g_m \left(R_C \parallel R_L\right).$$

The overall voltage gain (from source to load) is:

$$A_{vs} = \frac{v_o}{v_i}\frac{v_i}{v_s} = A_v \frac{R_i}{R_i + R_s} = A_{v0}\frac{R_L}{R_{RL} + R_o}\frac{R_i}{R_i + R_s} = -g_m R_C \frac{R_L}{R_L + R_o}\frac{R_i}{R_i + R_s}$$

The negative voltage gain indicates phase inversion.

Current Gain

The overall current gain of the amplifier is given by the transistor and two current dividers:

$$A_i = \frac{i_o}{i_i} = \frac{i_o}{i_c}\frac{i_c}{i_b}\frac{i_b}{i_i} = \frac{R_c}{R_c + R_L}\beta\frac{R_B}{R_B + r_{be}} \cong \beta$$

The circuit current gain is approximately equal to the transistor current gain for:
$R_B >> r_{be}$ and $R_C >> R_L$.

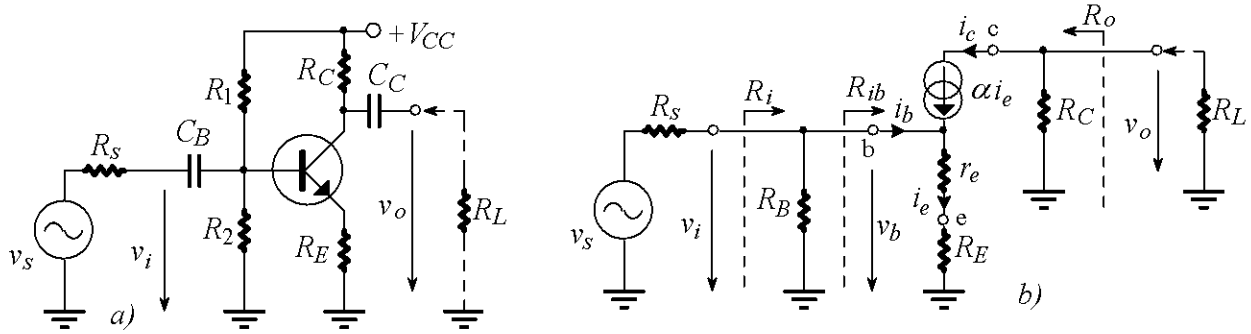
The Power Gain

The power gain is the product of the voltage gain and the current gain and it has a very high value (reduced by the two voltage dividers and by the two current dividers):

$$A_p = |A_v| \cdot A_i = g_m R_C \frac{R_L}{R_L + R_o} \frac{R_i}{R_i + R_s} \cdot \beta \frac{R_c}{R_c + R_L} \frac{R_B}{R_B + r_{be}}.$$

The Common-Emitter Amplifier with Unbypassed Emitter Resistance

Leaving the emitter resistance (or part of it) unbypassed provides us with an additional design parameter that can be used to improve some performance aspects of the CE circuit at the expense of a reduction in gain. Analysis can be performed by replacing the BJT by its simplified hybrid-π model. Let's consider the T model of BJT (ac model with r_e); the ac equivalent circuit is given in the next figure.



Input Resistance

Looking from the source to the amplifier you will see R_1 in parallel with R_2 (that is R_B) in parallel with the input resistance looking into the base of the transistor R_{ib}:

$$R_{ib} = \frac{v_b}{i_b} = \frac{v_i}{i_b} = \frac{i_e r_e + i_e R_E}{i_e/(\beta+1)} = (\beta+1)\cdot(r_e + R_E); \qquad R_i = R_1 \parallel R_2 \parallel R_{ib} = R_B \parallel R_{ib}$$

This first result says that: the input resistance looking into the base of a transistor is equal to the total resistance in its emitter multiplied by the factor (β+1); that is **the reflection rule from emitter to base**.

Voltage Gain

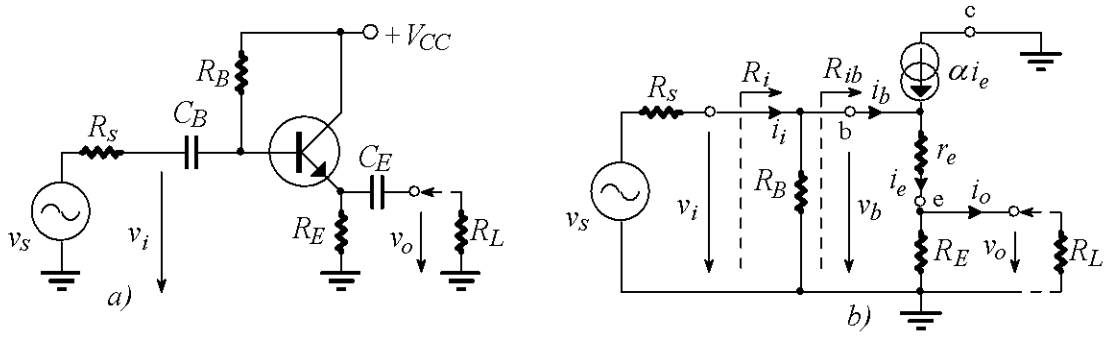
The voltage gain is the ratio of the total resistance in the collector to the total resistance in the emitter lead: $$A_v = \frac{v_o}{v_i} = \frac{-\alpha \cdot i_e (R_C \parallel R_L)}{i_e (r_e + R_E)} = -\frac{\alpha \cdot (R_C \parallel R_L)}{r_e + R_E} \cong -\frac{R_C \parallel R_L}{r_e + R_E}$$

The overall voltage gain can be obtained by multiplying A_v by the transmission from the source to the input (base): $$A_{vs} = \frac{v_o}{v_s} = \frac{v_o}{v_i}\frac{v_i}{v_s} = A_v \frac{R_i}{R_i + R_s} \cong -\frac{R_C \parallel R_L}{r_e + R_E}\frac{R_i}{R_i + R_s}$$

Comparison of the results with those of the CE amplifier indicates that leaving (part) of the emitter resistance unbypassed increases the input resistance and thus decrease the loss of signal strength in coupling the source to the amplifier input. The price paid for this improvement is a substantial reduction of voltage gain.

The Emitter Follower (Common-Collector Configuration)

The emitter follower is characterized by a high input resistance and a low output resistance (compared to CE configuration). It therefore is useful as an isolated or buffer amplifier to connect a high-resistance source to a low-resistance load.



Input Resistance

To obtain R_{ib} we use the reflection rule from emitter to base; the total resistance in the emitter lead is multiplied by (β+1): $R_{ib} = (\beta+1)\cdot(r_e + R_E \parallel R_L)$.

The input resistance is: $R_i = R_B \parallel R_{ib}$.

Voltage Gain

The output voltage v_o is equal to the emitter voltage and can be determined using the voltage divider rule: $v_o = \dfrac{R_e}{R_e + r_e} v_b = \dfrac{R_e}{R_e + r_e} v_i$;

With $R_e = R_E \parallel R_L$ being the ac equivalent resistance connected at the emitter terminal.

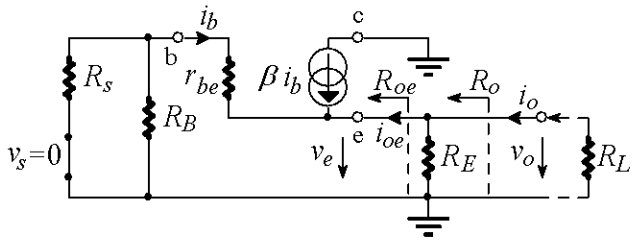
The voltage gain is: $A_v = \dfrac{v_o}{v_i} = \dfrac{R_e}{R_e + r_e}$. $A_v \cong 1$ for $r_e << R_E$.

The name emitter follower arises because the voltage at the emitter follows the input voltage. The voltage gain is less than unity but usually is close to unity (r_e is quite small, usually much smaller than R_e).

The signal analysis can be performed directly on the circuit – that is, with the equivalent circuit implicitly assumed.

Output Resistance

An alternative way of describing the performance of emitter follower is to specify the Thevenin equivalent circuit at the output. In the near figure it is represented the circuit used to compute the Thevenin output resistance: $R_O = \left.\dfrac{v_o}{i_o}\right|_{v_s=0}$ and the output resistance at the emitter lead: $R_{oe} = \left.\dfrac{v_e}{i_{oe}}\right|_{v_s=0}$.



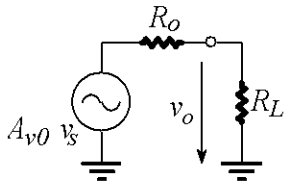
The emitter voltage and current are: $v_e(=v_o) = -i_b(R_s \parallel R_B + r_{be})$; $i_e(=-i_{oe}) = (\beta+1)\cdot i_b$.

The output resistance on the emitter lead is: $R_{oe} = \dfrac{-i_b\left(R_s \parallel R_B + r_{be}\right)}{-\left(\beta+1\right)\cdot i_b} = \dfrac{R_s \parallel R_B + r_{be}}{\beta+1}$

All resistances on the base side may be reflected to the emitter side after dividing their value by the factor (β+1) – that is **the reflection rule from base to emitter**.

The voltage gain from source to emitter (without load) and the overall voltage gain are:

$$A_{vs} = \frac{v_o}{v_s} = \frac{v_o}{v_i}\frac{v_i}{v_s} = \frac{R_E}{R_E + r_e}\frac{R_i}{R_i + R_s}, \qquad A_{vs} = A_{v0}\frac{R_L}{R_L + R_o}.$$



The overall voltage gain was computed with the Thevenin equivalent of the voltage follower.

Applications

S7 – P1. The transistor in the circuit of figure has $\beta = 100$ and $V_{BE} = 0.7\ \text{V}$.

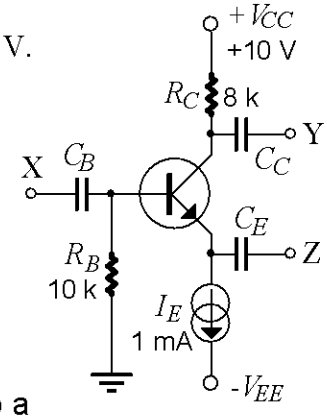
a) Find the dc voltages at the base, emitter and collector;

b) Find g_m and r_{be} (assume $V_T = 25\ \text{mV}$).

c) If terminal Z is connected to ground, X connected to signal source v_i, and Y to an $8\ \text{k}\Omega$ load resistance, use the small signal model to find the voltage gain $A_v = v_y / v_i$ (CE configuration).

d) If Y is connected to ground, X to an input to signal source v_i, and Z to a load resistance of $1\ \text{k}\Omega$, find the voltage gain $A_v = v_z / v_i$ (CC configuration – voltage follower).

e) If X is connected to ground, Z to an input signal source v_i, and Y to a load resistance of $8\ \text{k}\Omega$, find the voltage gain $A_v = v_y / v_i$ (common-base configuration).



a) $I_C \cong I_E = 1\,\text{mA}, \quad I_B = \dfrac{I_C}{\beta} = 0.01\,\text{mA}, \quad V_B = -R_B I_B = -10k \cdot 0.01m = -0.1\,\text{V},$

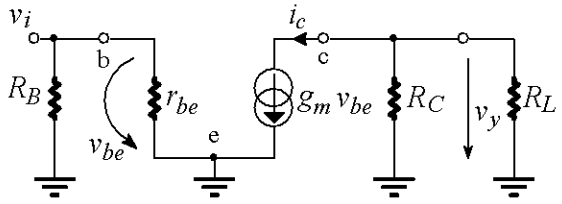
$V_C = V_{CC} - R_C I_C = 10 - 8k \cdot 1m = 2\,\text{V}, \quad V_E = V_B - V_{BE} = -0.1 - 0.7 = -0.8\,\text{V}.$

b) $g_m = \dfrac{I_C}{V_T} = \dfrac{I_C}{25m} = 40 I_C = 40 \cdot 1m = 40\,\text{mA/V}; \quad r_{be} = \dfrac{\beta}{g_m} = \dfrac{100}{40m} = 2.5\,\text{k}\Omega.$

c) $v_y = -i_c \cdot \left(R_C \parallel R_L\right) = -g_m v_{be} R_c$; $v_i = v_{be}$ and

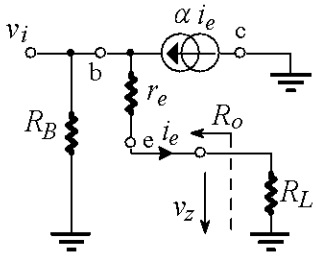
$A_v = \dfrac{v_y}{v_i} = -g_m R_c = -40m \cdot 4k = -160$

(with $R_c = R_C \parallel R_L = 8k \parallel 8k = 4\,\text{k}\Omega$).



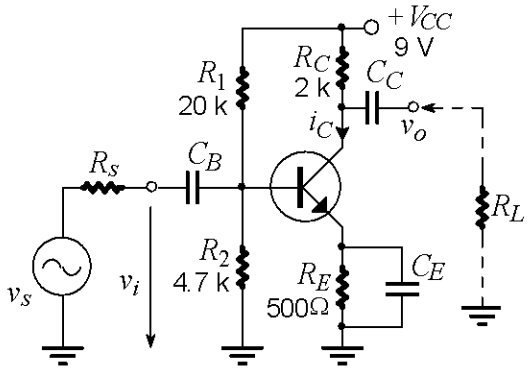
d) $v_i = i_e r_e + i_e R_L = i_e\left(r_e + R_L\right); \qquad v_z = i_e R_L$ and

$A_v = \dfrac{v_z}{v_i} = \dfrac{R_L}{R_L + r_e} = \dfrac{1k}{1k + 25} = 0.976$ (with $r_e = \dfrac{V_T}{I_C} = \dfrac{1}{g_m} = 25\,\Omega$).



e) $A_v = \dfrac{v_y}{v_i} = g_m R_c = 40m \cdot 4k = 160.$

S7 – P2. *a)* Determine the voltage gain and the input and output resistances for the amplifier in figure; consider: $I_C = 2\,\text{mA}$, $\beta = 200$, $V_T = 25\,\text{mV}$, ($V_{BE} = 0.7\,\text{V}$).
b) Assume that a $600\,\Omega$, $10\,\text{mV}$ (rms) voltage source is driving the amplifier and a $2\,\text{k}\Omega$ load is connected at the output. Determine the overall gain and the output rms voltage.
c) If the emitter capacitor opens, what is the new value of voltage gain and the overall gain (point *b* conditions).
d) Redesign the circuit with an additional resistance in the emitter to get a voltage gain of 10 (for no load conditions) keeping the same Q point.



Find the voltages at all nodes and the currents through all branches in the circuit for.

a) $V_B = \dfrac{R_2}{R_1+R_2}V_{CC} = \dfrac{4.7k}{24.7k}9 = 1.7\,\text{V},\ I_E = \dfrac{V_E}{R_E} = \dfrac{V_B - V_{BE}}{R_E} = \dfrac{1}{0.5k} = 2\,\text{mA},$

$I_B = \dfrac{I_E}{\beta} = 0.01mA << I_{Div} = 0.36mA\,,\ V_{CE} = V_{CC} - R_C I_C - V_E = 9 - 4 - 1 = 4\,\text{V}.$

Transistor parameters are: $g_m = \dfrac{I_C}{V_T} = 40 I_C = 80\,\text{mA/V};$ $\qquad r_{be} = \dfrac{\beta}{g_m} = \dfrac{200}{80m} = 2.5\,\text{k}\Omega.$

Amplifier parameters are: $A_{v0} = -g_m R_c = -80m \cdot 2k = -160\,;\ R_o = R_C = 2\,\text{k}\Omega;$

$R_B = R_1 \parallel R_2 = 20k \parallel 4.7k = 3.2\,\text{k}\Omega,\ R_i = R_B \parallel r_{be} = 3.2k \parallel 2.5k = 1.4\,\text{k}\Omega.$

b) $V_i = \dfrac{R_i}{R_i+R_s}V_s = \dfrac{1.4k}{1.4k+0.6k}10m = 7\,\text{mV};\ V_o = |A_{v0}| \cdot V_i \dfrac{R_L}{R_L+R_o}\,;\ A_v = \dfrac{V_o}{V_i} = A_{v0}\dfrac{R_L}{R_L+R_o}\,;$

$A_{vs} = \dfrac{V_o}{V_s} = \dfrac{V_o}{V_i}\dfrac{V_i}{V_s} = A_{v0}\dfrac{R_L}{R_L+R_o}\dfrac{R_i}{R_i+R_s} = -160\dfrac{2k}{2k+2k}\dfrac{1.4k}{1.4k+0.6k} = -56\,;\ V_o = V_s|A_{vs}| = 560\,\text{mV};$

$V_o = V_s|A_{vs}| = 10m \cdot 56 = 560\,\text{mV};$ $\qquad$ or $\qquad V_o = V_i|A_v| = 7m \cdot 160 \cdot \dfrac{2k}{2k+2k} = 7m \cdot 80 = 560\,\text{mV}.$

c) $A_{v0} = -\dfrac{R_C}{R_E + r_e} = -\dfrac{2k}{500+12.5} = -3.9\,,$ $\quad$ (with $r_e = 1/g_m = 1/80m = 12.5\,\Omega$);

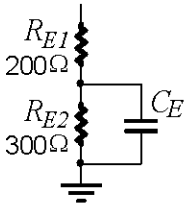
$R_{ib} = r_{be} + (\beta+1)R_E = 2.5k + 201 \cdot 0.5k = 103\,\text{k}\Omega;\ R_i = R_B \parallel R_{ib} = 3.2k \parallel 103k = 3\,\text{k}\Omega;$

$A_{vs} = A_{vo}\dfrac{R_L}{R_L+R_o}\dfrac{R_i}{R_i+R_s} = -3.9\dfrac{2k}{2k+2k}\dfrac{3k}{3k+0.6k} - 3.9 \cdot 0.5 \cdot 0.83 = -1.62$ (34.6 time lower).

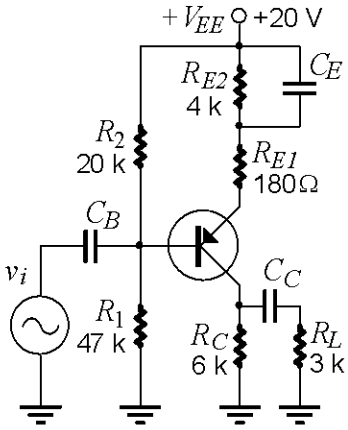
d) Split the emitter resistance in two parts (see figure), one bypassed by the emitter capacitor (R_{E1}) and one unbypassed (R_{E2}); theirs sum should be equal to the previous emitter resistance to keep the same Q point. The unbypassed part gives the gain:

$|A_{v0}| \cong \dfrac{R_C}{R_{E1}} = 10\,;$ $\qquad R_{E1} \cong \dfrac{R_C}{|A_{v0}|} = \dfrac{2k}{10} = 200\,\Omega;$

$R_{E2} = R_E - R_{E1} = 500 - 200 = 300\,\Omega.$



S8 – P1. *a)* Calculate the voltage gain from base to collector for the amplifier shown in figure. If the ac source signal is a sine wave with 0,1 V peak, what does $\hat{V}_c$ equal? And $\hat{V}_e$? (Assume $V_{EB}=0.7\text{ V}$ and $V_T=25\text{ mV}$.)
b) If the collector coupling capacitor opens, what is the new value of voltage gain (from base to collector)?
c) If the collector capacitor shorts what effect will have on the *dc* operation and on the *ac* operation?
d) If the base coupling capacitor shorts what will do this to the *dc* operation (assume $V_{EC\,\text{sat}}=0.3\text{ V}$).



a) ***dc*** analysis: $V_{R2}\cong\dfrac{R_2}{R_1+R_2}V_{EE}=\dfrac{20k}{20k+47k}20=6\text{ V},$

$$I_E=\frac{V_{R_E}}{R_E}=\frac{V_{R2}-V_{EB}}{R_E}=\frac{5.3}{4.18k}=1.27\text{ mA},\quad\left(I_{R2}=\frac{V_E}{R_1+R_2}=0.3mA=0.24I_E\right),$$

$V_{EC}=V_{EE}-V_{R_E}-R_CI_C=20-5.3-6k\cdot1.27m=7.1\text{ V}$ (BJT is in the active regime).

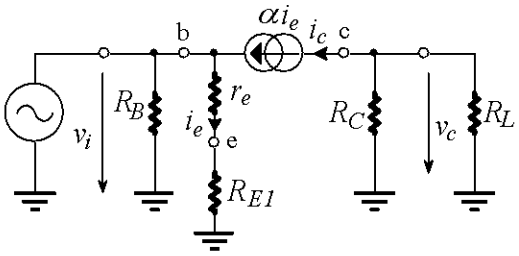
Transistor parameters are: $r_e=\dfrac{V_T}{I_C}=\dfrac{25m}{1.27m}\cong20\,\Omega;\qquad\alpha\cong1.$

ac analysis: $v_b=i_e(r_e+R_{E1})$

$v_c=-i_c(R_c\parallel R_L)\cong-i_e(R_c\parallel R_L);$

$$\hat{V}_c=\left|\frac{-i_c(R_c\parallel R_L)}{i_e(r_e+R_{E1})}\right|\cdot\hat{V}_b=\frac{R_c\parallel R_L}{r_e+R_{E1}}\cdot\hat{V}_b=\frac{2k}{20+180}0.1=1\text{ V}.$$

$$\hat{V}_e=\frac{R_{E1}}{r_e+R_{E1}}\cdot\hat{V}_b=\frac{180}{20+180}0.1=0.09\text{ V}.$$



b) R_L is an open-circuit (w/o R_L): $A_{v0}=\dfrac{v_c}{v_b}=-\dfrac{R_L}{r_e+R_{E1}}=-\dfrac{6k}{20+180}=-30.$

c) ***dc*** analysis (R_L is in parallel with R_C): $V_C=I_C(R_C\parallel R_L)=1.27m\cdot2k=2.54\text{ V},$

$V_{EC}=V_{EE}-V_{R_E}-V_C=20-2.54-5.3=12.2\text{ V}$; instead of 7.1 V; ***ac*** operation is the same.

d) ***dc*** analysis: $V_B=0;\qquad V_E=V_{EB}=0.7\text{ V},$ For the transistor in active regime,

the emitter current would be: $I_E=\dfrac{V_{EE}-V_E}{R_E}=\dfrac{19.3}{4.18k}=4.6\text{ mA}.$

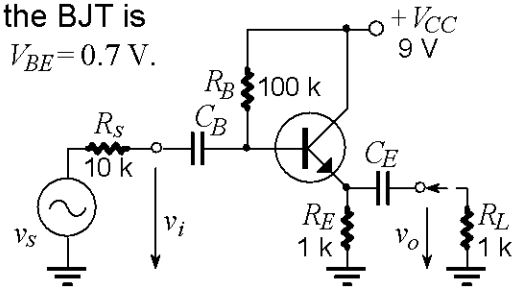
The maximum possible collector current is: $I_{C\max}=\dfrac{V_{EE}}{R_E+R_C}=\dfrac{20}{4.18k+6k}=1.96\text{ mA};$

(with the transistor in saturation; between active mode and saturation mode). Because $I_E>I_{C\max}$ the transistor is in saturation and $V_{EC}=V_{ECsat}=0.3\text{ V};$

The collector current is: $I_C=\dfrac{V_C}{R_C}=\dfrac{V_E-V_{ECsat}}{R_C}=\dfrac{0.7-0.3}{6k}=0.067\text{ mA}.$

The base current is: $I_B=I_E-I_C=4.6m-0.67m\cong3.9\text{ mA}.$

S8 – P2. For the emitter follower circuit shown in figure, the BJT is specified to have β values in the range of 100 to 500 and $V_{BE}=0.7\ \text{V}$.



For the two extreme value of β find:

a) The bias point: I_E and V_E;

b) The input resistance R_i;

c) The overall voltage gain $A_{vs}=v_o/v_s$.

a) $$I_E=\frac{V_{CC}-V_{BE}}{R_E+\dfrac{R_B}{\beta+1}}=\frac{9-0.7}{1k+\dfrac{100k}{101...501}}=(4.17...6.92)\text{mA},$$

$$V_E=R_E I_E=(4.17...6.92)\ \text{V}.$$

$$r_e=\frac{V_T}{I_E}=\frac{25m}{(4.17...6.92)m}=(6...3.6)\Omega;$$

b) $$R_{ib}=(\beta+1)\cdot(r_e+R_E\parallel R_L)=(101...501)\cdot(6...3.6+500)=51...252\,\text{k}\Omega;$$

$$R_i=R_B\parallel R_{ib}=33.8...71.6\,\text{k}\Omega.$$

c) $$R_e=R_E\parallel R_L=500\,\Omega;\qquad A_{vs}=\frac{v_o}{v_s}=\frac{v_o}{v_i}\frac{v_i}{v_s}=\frac{R_e}{R_e+r_e}\frac{R_i}{R_i+R_s}=\frac{1}{1+\dfrac{r_e}{R_e}}\cdot\frac{1}{1+\dfrac{R_s}{R_i}};$$

$$A_{vs}=\frac{1}{1+\dfrac{6...3.6}{500}}\cdot\frac{1}{1+\dfrac{10k}{(33.8...71.6)k}}=(0.988...0.993)\cdot(0.77...0.877)=0.76...0.87\,.$$