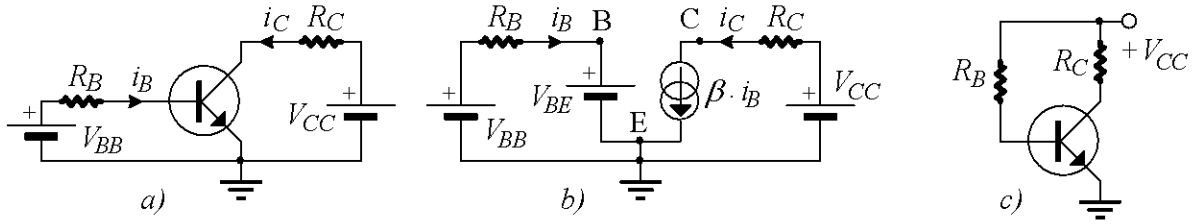
DC Analysis of Transistor Circuits

We will use the simple constant V_D model. Specifically, we will assume $v_{BE} = V_D\,(= 0.6 \ldots 0.7\,\mathrm{V})$ (or $v_{EB} = V_D$ for pnp transistors) irrespective of the exact value of current. This approximation can be refined using the exponential equation (BJT basic equation).

Biasing the BJT for Discrete Circuit Design

The biasing problem is that of establishing a constant *dc* current in the emmiter of the BJT (simply called „transistor current"). This current has to be calculable, predictible and insensitive to variations (in temperature and to the large variations in the value of β – encountered among transistors of the same type).

Base Bias



$$I_B = \frac{V_{BB} - V_{BE}}{R_B}, \qquad I_C = \beta \cdot I_B, \quad V_{CE} = V_{CC} - R_C I_C = V_{CC} - \beta \cdot I_B R_C .$$

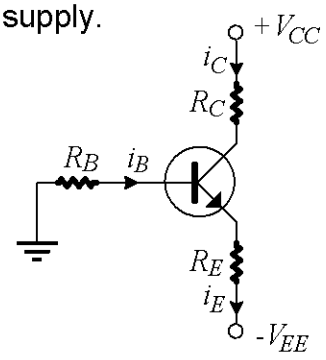
Equations for I_C and V_{CE} include β. The disadvantage is that β variations cause both I_C and V_{CE} to change, that making the base-bias circuit beta-dependent. β varies with temperature and there can be a spread of values from one device to another of the same type.
A more practical method of base bias is to use V_{CC} as a single power source. To simplify the schematics, the battery symbol can be omitted and replaced by a line terminator with a voltage indicator, as indicated on the right part of the previous figure (c).

Emitter Bias

This type of bias circuits uses both a positive and a negative power supply.
By applying KVL to the emitter-base loop we get:

$V_{EE} = I_B R_B + V_{BE} + I_E R_E$; Since $I_B = \frac{I_E}{\beta + 1}$: $I_E = \frac{V_{EE} - V_{BE}}{R_E + \frac{R_B}{\beta + 1}}$.

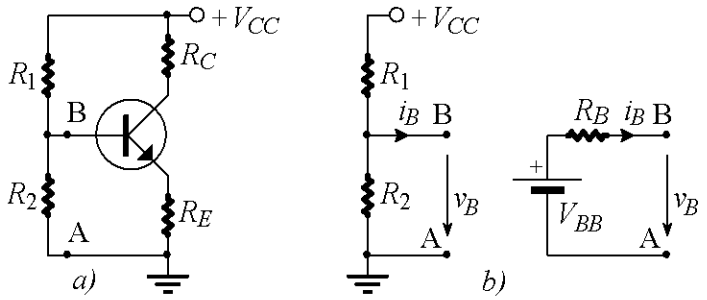
When $R_E >> \frac{R_B}{\beta + 1}$, equation reduced to $I_E = \frac{V_{EE} - V_{BE}}{R_E}$.



I_E is essentially independent of β. From C-E loop we get:
$V_{CE} = V_{CC} + V_{EE} - (R_C + R_E) \cdot I_E$.
The emitter bias provides a reasonable stable bias point, but needs two power supplies.

Voltage-Divider Bias

The voltage divider bias is the most widely used arrangment for linear transistor circuits. A bias voltage at the base is developed by a resistor voltage-divider. The voltage divider network can be replaced by its Thevenin equvalent circuit: $V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC}$, $R_B = R_1 \| R_2$.



$V_{BB} = I_B R_B + V_{BE} + I_E R_E$, $I_B = \frac{I_E}{\beta + 1}$ and $I_E = \frac{V_{BB} - V_{BE}}{R_E + \frac{R_B}{\beta + 1}}$. To make I_E insensitive to β and temperature variations, we design the circuit to satisfy the following two conditions: $V_{BB} >> V_{BE}$ and $R_E >> \frac{R_B}{\beta + 1}$. The 2nd condition means that we want to make the base voltage independent of the value of β. This will be satisfied if the current in the divider is made much larger than the base current: $I_{Div}\left(\cong \frac{V_{CC}}{R_1 + R_2} \right) > 10 \cdot I_{B\max}$ (with $I_{B\max} = \frac{I_C}{\beta_{\min}}$).

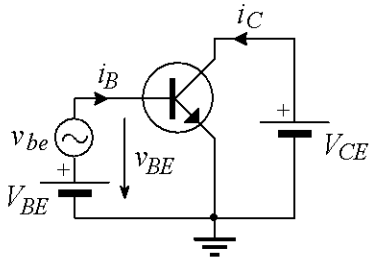
Alternatively we can select the divider resistances such that the divider current to be:

$$I_{Div} \geq 0.1 \cdot I_E .$$

Transistor ac Equivalent Circuits

Consider the conceptual circuit given in the next figure. For the *dc* analisys suppress the ac source, $v_{be} = 0$.

We have the *dc* currents: $I_C = I_S \exp \frac{V_{BE}}{V_T}$ and $I_B = \frac{I_C}{\beta}$.



Transconductance

The transconductance is the ratio of the signal current in the collector to the corresponding base-emitter signal voltage: $g_m = \frac{di_C}{dv_{BE}} = \frac{i_c}{v_{be}}$.

With the signal v_{be} applied, the total instantaneous base-emiter voltage (*dc* + *ac*) becomes: $v_{BE} = V_{BE} + v_{be}$.

Correspondingly, the collector current becomes:

$i_C = I_S \exp \frac{(V_{BE} + v_{be})}{V_T} = I_S \exp \frac{V_{BE}}{V_T} \cdot \exp \frac{v_{be}}{V_T} = I_C \exp \frac{v_{be}}{V_T}$; If $v_{be} << V_T$, we may approximate:

$i_C \cong I_C\left(1+\frac{v_{be}}{V_T}\right)$. (The exponential expanded in a series and the first two terms retained.)

This approximation, which is valid only for v_{be} less than about $10\ \mathrm{mV}$, is referred to as "**the small-signal approximation**": $v_{be} \le 10\mathrm{mV}$.

Under this approximation the total collector current signal component can be rewritten:

$i_C = I_C + \frac{I_C}{V_T}v_{be} = I_C + i_c$. The collector current signal component is: $i_c = \frac{I_C}{V_T}v_{be} = g_m v_{be}$.

The transconductance of a BJT under small signal approximation is: $g_m = \frac{I_C}{V_T}$.

We observe that the transconductance of the BJT is directly proportional to the collector bias current I_C. To obtain a constant, predictable value for g_m we need a constant, predictable I_C.

A graphical interpretation of transconductance is: $g_m = \left.\frac{di_C}{dv_{BE}}\right|_{I_C}$; that is the slope of the i_C-v_{BE} characteristic curve at $i_C = I_C$.

The analysis above suggests that the transistor behave as a voltage-controlled current source. The input port is between base and emitter and the output port is between collector and emitter.

The Input Resistance at the Base

To determine the resistance seen by the signal source, we first evaluate the total base current: $i_B = \frac{i_C}{\beta} = \frac{I_C}{\beta} + \frac{I_C}{\beta \cdot V_T}v_{be} = I_B + i_b$.

The signal component i_b is given by: $i_B = \frac{1}{\beta}\frac{I_C}{V_T}v_{be} = \frac{g_m}{\beta}v_{be}$.

The small-signal input resistance between base and emitter, looking into the base, r_π defined as $r_\pi = \frac{v_{be}}{i_b}$ is: $r_\pi = \frac{\beta}{g_m}$.

The r_π is directly dependent on β and is inversely proportional to the bias current I_C.

An alternate expression for r_π is: $r_\pi = \frac{V_T}{I_B}$.

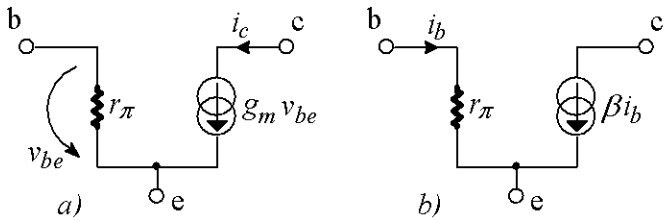
The Hibrid π Model

For small-signals, the BJT can be represented by the equivalent circuit shown in the left part of the next figure.

The equivalent circuit apply at a particular bias point, since the two parameters g_m and r_π depend on the value of I_C. Since the output current can be rewritten:

$$i_c = g_m v_{be} = g_m r_\pi i_b = \beta \cdot i_b,$$

the equivalent circuit model can be converted to the current-controlled current source form (the right part of next figure).



This equivalent circuit model is called the "simplified hybrid-π model".
This model applies to both *npn* and *pnp* transistor with **no change in polarity required**.

The Emitter Resistance

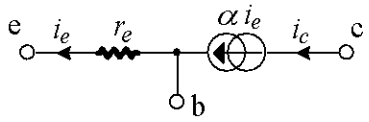
The total emitter current i_E can be determined by equation:

$$i_E = \frac{i_C}{\alpha} = I_E + i_e; \qquad i_e = \frac{I_C}{\alpha \cdot V_T} v_{be} = \frac{I_E}{V_T} v_{be}.$$

This relationship can be expressed in the form: $i_e = \frac{v_{be}}{r_e}$, where r_e, called "emitter resistance": $r_e = \frac{v_{be}}{r_e} = \frac{V_T}{I_E} = \frac{\alpha}{g_m} \cong \frac{1}{g_m}$ does not depend on I_C.

An useful interpretation for r_e is that it is the resistance between base and emitter looking into emitter and $r_\pi = (\beta + 1) \cdot r_e$.

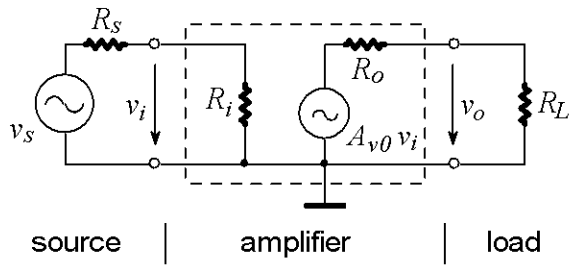
An alternative small-signal model that explicitelly employs r_e is given in the next figure.



Use of Small-Signal Equivalent Circuits

All curents and voltages in a circuit consist of a *dc* bias component and an *ac* signal component. We may use the superposition theorem for *ac-dc* circuits and consider the two component separately.
From the signal point of view the transistor may be replaced by one of the *ac* equivalent models.
If one is interested only in obtaining approximate values using first order models, it is far quicker to analyse simple circuits with the model implicitely assumed.

The Voltage Amplifier Model



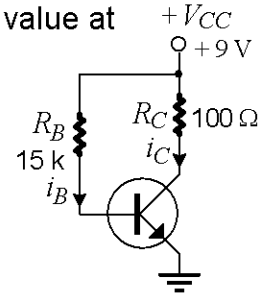
(To be completed…) – Course notes or Romanian book (Modelul amplificatorului de tensiune).

Applications

S6 – P1. The data sheet for a particular transistor specifies a minimum β of 50 and a maximum β of 130, $v_{BE}=V_D=0.7$ V and $V_{CEsat}=0.3$ V.

a) What range of Q point can be expected if an attempt is made to mass-produce the circuit in figure. Is this range acceptable?

b) The base bias circuit is subject to a temperature variation from 0 to 70°C. The β decreases by 20% at 0°C and increases by 35% at 70°C from its nominal value at 25°C. Compute the Q point limits for the specified temperature range.



a) $I_B=\dfrac{V_{CC}-v_{BE}}{R_B}=\dfrac{V_{CC}-V_D}{R_B}=\dfrac{9-0.7}{15k}=0.553\,\text{mA}.$

$I_C=\beta\cdot I_B=(50...130)\cdot 0.553m=28...72\ \text{mA}.$

$V_{CE}=V_{CC}-R_C I_C=9-0.1k\cdot(28...72)m=6.2...1.8\ \text{V}.$

This range of Q point is not acceptable because of the big variations of I_C and V_{CE}.

b) $\beta_{\min}=0.8\cdot 50=40$, $\beta_{\max}=1.35\cdot 130=175.5$;

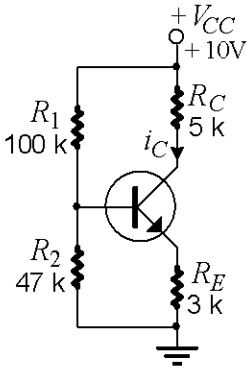
$I_{C\min}=\beta_{\min}\cdot I_B=40\cdot 0.553m=22\,\text{mA}$, $V_{CE\max}=V_{CC}-R_C I_{C\max}=9-0.1k\cdot 22m=6.8\,\text{V}.$

$I_{C\max}=\beta_{\max}\cdot I_B=175.5\cdot 0.553m=97\,\text{mA}$, $V_{CE\min}=V_{CC}-R_C I_{C\max}=9-0.1k\cdot 97m=-0.7\,\text{V}.$

A negative value for V_{CE} is not possible; it means that the transistor is saturated. The maximum I_C and maximum β in active mode are:

$I_{C\max}=\dfrac{V_{CC}-V_{CEsat}}{R_C}=\dfrac{9-0.3}{0.1k}=87\,\text{mA}$, $\beta=\dfrac{I_{C\max}}{I_B}=\dfrac{87m}{0.553m}=157$. For $\beta>157$ the circuit will saturate the BJT and the corresponding Q point is: $I_C=87$ mA and $V_{CE}=V_{CEsat}=0.3$ V.

S6 – P2. Consider the circuit of figure, *a)* initially for infinite β, *b)* then for $\beta=100$. Find the voltages at all nodes and the currents through all branches in the circuit for $v_{BE}=V_D=0.7$ V.



a) $V_B=\dfrac{R_2}{R_1+R_2}V_{CC}=3.2\,\text{V}$, $V_E=V_B-V_{BE}=2.5\,\text{V}.$

$I_E=\dfrac{V_E}{R_E}=\dfrac{2.5}{3k}=0.83\,\text{mA}$, $I_B=\dfrac{I_E}{\beta}=\dfrac{0.83m}{\infty}=0$,

$I_C=I_E-I_B=I_E=0.83\,\text{mA}$, $V_C=V_{CC}-R_C I_C=10-5k\cdot 0.83m=5.83\,\text{V}.$

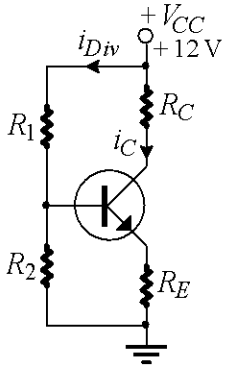
b) $V_{BB}=3.2\,\text{V}$, $R_B=R_1\|R_2=32\,\text{k}\Omega$,

$I_E=\dfrac{V_{BB}-V_{BE}}{R_E+R_B/(\beta+1)}=\dfrac{2.5}{3k+32k/101}=0.754\,\text{mA}$, $I_B=I_E/(\beta+1)=7.46\,\mu\text{A}$,

$I_C=\beta\cdot I_B=0.746\,\text{mA}$, $V_B=V_{BB}-R_B I_B=3.2-32k\cdot 7.46\mu=2.96\,\text{V}$,

$V_E=R_E I_E=3k\cdot 0.754m=2.26\,\text{V}$, $V_C=V_{CC}-R_C I_C=10-5k\cdot 0.746m=6.27\,\text{V}.$

S6 – P3. *a)* Design the bias network of the circuit in figure to establish a current $I_C = 1\,\text{mA}$ whith $v_{BE} = V_D = 0.7\,\text{V}$, using a power supply $V_{CC} = 12\,\text{V}$.
b) Calculate the expected range of I_C and V_{CE} if the transistor β is in the range of 100 to 300.



Hints: 1. Allocate one-third of the supply voltage to the votage drop across R_2 and another third to the voltage drop across R_C, leaving one-third for possible signal swing at the collector.
2. Consider the current in the divider at least a tenth of the collector current.

a) $V_B = \dfrac{V_{CC}}{3} = 4\,\text{V}, \quad V_E = V_B - V_{BE} = 3.3\,\text{V}, \quad R_E = \dfrac{V_E}{I_E} \cong \dfrac{V_E}{I_C} = \dfrac{3.3}{1m} = 3.3\,\text{k}\Omega,$

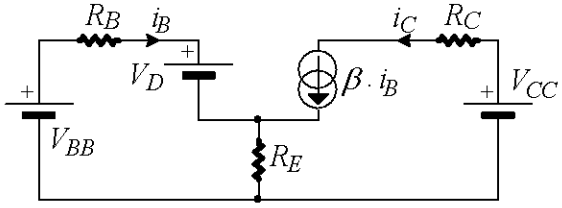
$\left(I_E = I_C + I_B = I_C + \dfrac{I_C}{\beta} = I_C\left(1 + \dfrac{1}{\beta}\right) \cong I_C \right) \qquad R_C = \dfrac{V_{CC} - V_C}{I_E} = \dfrac{V_{CC}/3}{I_C} = \dfrac{4}{1m} = 4\,\text{k}\Omega,$

$I_{Div} = \dfrac{I_C}{10} = 0.1\ \text{mA}, \ R_1 + R_2 \cong \dfrac{V_{CC}}{I_{Div}} = \dfrac{12}{0.1m} = 120\,\text{k}\Omega,$

$V_B (= V_{BB}) \cong \dfrac{R_2}{R_1 + R_2} V_{CC} \Rightarrow R_2 = \dfrac{V_B}{V_{CC}}(R_1 + R_2) = \dfrac{4}{12} 120k = 40\,\text{k}\Omega, \quad R_1 = (R_1 + R_2) - R_2 = 80\,\text{k}\Omega.$

We could, of course, obtain a value much closer to the desired I_C by designing with exact equations (considering R_B that gives different values for V_B and V_{BB}). However, since our work is based on first order models, it does not make sense to strive for accuracy better than about 10%.

b)



$V_{BB} = \dfrac{R_2}{R_1 + R_2} V_{CC} = 4\,\text{V}, \ R_B = R_1 \| R_2 = 27\,\text{k}\Omega,$

$I_C = \beta \dfrac{V_{BB} - V_{BE}}{R_B + R_E \cdot (\beta + 1)} = \dfrac{(100...300) \cdot 3.3}{27k + 3.3k \cdot (101...301)} = 0.917...0.971\text{mA},$

$V_{CE} \cong V_{CC} - (R_C + R_E) \cdot I_C = 12 - (4k + 3.3k) \cdot (0.917...0.971)m = 5.31...4.91\,\text{V}.$

The current variation is: $\dfrac{\Delta I_C}{I_{Cmed}} = \dfrac{0.054}{0.944} = 5.7\,\%$ for a current gain variation of

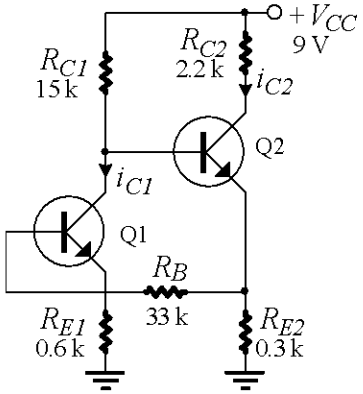
$\dfrac{\Delta\beta}{\beta_{med}} = \dfrac{200}{200} = 100\,\%$; the variation is reduced significantly (approximately 18 times).

S6 – P4. The transistors in figure have β=300, V_{BE1}=V_{D1}=0.6 V and V_{BE2}=V_{D2}=0.7 V. What are I_C and V_{CE} at the Q point for the transistor.

We assume I_C= I_E (the currents differ by about 0.3% for the given β). We neglect also the base curents in respect to the collector currents; after the currents are determined, we verify these assumptions. We need two equations (KVL) to determine the two collector currents:

(a) $V_{CC} = R_{C1}I_{C1} + V_{BE2} + R_{E2}I_{C2}$, *(b)* $R_{E2}I_{C2} = R_B \frac{I_{C1}}{\beta} + V_{BE1} + R_{E1}I_{C1}$.

By replacing the 2nd equation *(b)* in the 1st one *(a)* we get:



$V_{CC} = R_{C1}I_{C1} + V_{BE2} + R_B \frac{I_{C1}}{\beta} + V_{BE1} + R_{E1}I_{C1}$ and

$$I_{C1} = \frac{V_{CC} - V_{BE1} - V_{BE2}}{R_{C1} + R_{E1} + \frac{R_B}{\beta}} = \frac{9 - 0.6 - 0.7}{15k + 0.6k + \frac{33k}{300}} = 0.49\,\text{mA}.$$

$$I_{C2} = \frac{V_{CC} - R_{C1}I_{C1} - V_{BE2}}{R_{E2}} = \frac{9 - 15k \cdot 0.49m - 0.7}{0.3k} = 3.17\,\text{mA}.$$

We check the currents: $I_{B1} << I_{C2}$ and $I_{B2} << I_{C1}$:

$I_{B1} = \frac{I_{C1}}{\beta} = \frac{490\mu}{30} = 1.63\,\mu\text{A}$, $\frac{I_{C2}}{I_{B1}} = \frac{3170\mu}{1.63\mu} = 1945$, so that

$I_{B1} << I_{C2}$ (1940 times lower);

$I_{B2} = \frac{I_{C2}}{\beta} = \frac{3170\mu}{300} = 10.6\,\mu\text{A}$, $\frac{I_{C1}}{I_{B2}} = \frac{490\mu}{10.6\mu} = 46$, so that $I_{B2} << I_{C1}$ (46 times lower).

Finnaly, the C-E voltages are computed:

$V_{CE2} \cong V_{CC} - (R_{C2} + R_{E2}) \cdot I_{C2} = 9 - (2.2k + 0.3k) \cdot 3.17m = 1.075\,\text{V}$;

$V_{CE1} = V_{BE2} + R_B \frac{I_{C1}}{\beta} + V_{BE1} = 0.7 + 33k \frac{0.49m}{300} + 0.6 = 1.354\,\text{V}.$