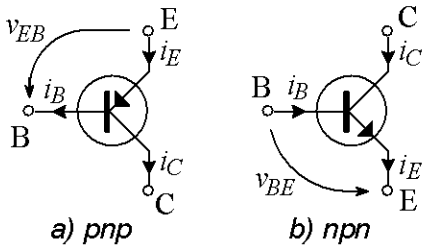
The Bipolar Junction Transistor

The bipolar junction transistor (BJT) consists on tree semiconductor regions called: emitter, base and collector, separated by two *pn* junctions that share a common region, the base, between them. The base material is very narrow and lightly doped compared to the heavily doped emitter. The BJT can be a "*npn*" or a "*pnp*" type.
Depending on the bias condition (forward or reverse) of the two *pn* junctions, four different modes of operation of the BJT are possible.



EBJ	CBJ	Mode of operation
Reverse	Reverse	Cutt-off
Forward	Reverse	Normal Active
Forward	Forward	Saturation
Reverse	Forward	Inverse Active

The polarity of the device – *npn* or *pnp* – is indicated by the direction of the arrowhead on the emitter (that points in the EB junction direction). This arrowhead points in the direction of normal current flow in the transistor.
The active mode is the one used if the transistor is to operate for linear applications (e.g. amplification). Switching applications utilize both the cutoff and the saturation modes.

The Physical Basis of Transistor Operation

Injection, Diffusion and Collection – figure
(To be written…) – Course notes or Romanian book (Construcția şi funcționarea tranzistorului).

An *npn* transistor in the active mode of operation has: $v_{BE}>0$ and $v_{CB}>0$.
The BJT works by combining injection at the emitter-base junction (that is forward bias) with collection at the collector-base junction (that is reverse biased). By doping the emitter region much more heavily than the base, most of the injection carrier is made to occur into the base side of the emitter-base junction (through electrons). The concentration gradient of minority electrons across the base produces a diffusive flow of electrons from the emitter end (where they are in excess) to the collector end, where they are swept into the collector region. Nearly all electrons entering the base from the emitter reach the collector (because the base is very thin and the percentage of electrons that recombines with holes will be quite small). That is expressed by the relation between collector and emitter currents:

$$i_C = \alpha \cdot i_E \text{ with } \alpha = 0.98...0.998$$

α is called the common-base current gain; α is smaller than, but very close to unity.

Equivalent Circuit Models

The emitter current is the current in a forward bias junction (EBJ). One of the BJT model consists on a diode between base and emitter (EBJ) and a current source in collector; this is the model of the BJT controlled through emitter; with the base being common to input port (E-B) and output port (C-B), as indicated on the left side of the next figure.

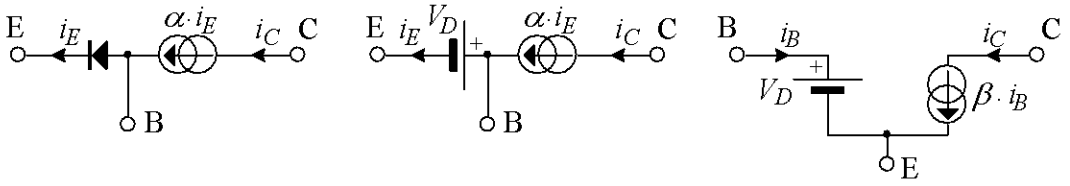


Figure – *Equivalent circuit models for npn type BJT.*

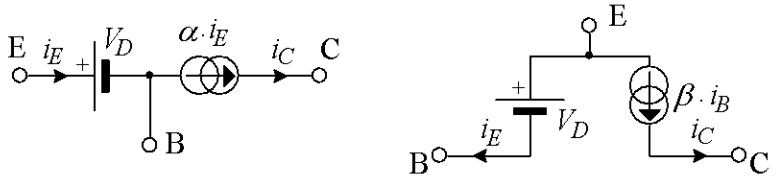
The collector current can be expressed as a function of emitter-base voltage; this is the so-called "**Basic equation of BJT**":

$$i_C = I_S \exp \frac{v_{BE}}{V_T}.$$

I_S is the saturation current (or current scale factor) of EBJ; it is proportional to the area of EBJ and inversely proportional to the base width, its value is in the nA range.
V_T is the thermal voltage (same as for the diodes) with a value of $25\ \mathrm{mV}$ for $17\ ^{o}\mathrm{C}$.
In order to simplify the nonlinear model (given by the nonlinear diode) one can consider the linear model of the forward bias diode and replace the diode by a voltage source V_D (with a usual value of 0.6 to $0.7\ \mathrm{V}$); this model is given in the middle of the previous figure.
If the transistor is controlled through the base it will be useful to express the collector current as a function of base current. One can start from the BJT continuity equation (KCL over the BJT) and replace i_E from the collector-emitter current relationship:

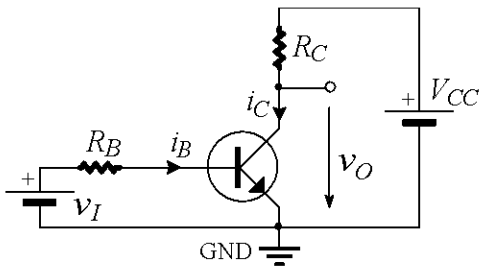
$$i_E = i_C + i_B,\ \frac{i_C}{\alpha} = i_C + i_B,\ i_C \frac{1-\alpha}{\alpha} = i_B,\ i_C = \frac{\alpha}{1-\alpha} i_B = \beta \cdot i_B.$$

$\beta = \dfrac{\alpha}{1-\alpha}$ is called the common-base current gain (with values of 50 to 500 – compute by α limits); β values are usually from 100 to 300. The model of BJT controlled through base is given in the right side of the previous figure.
The *pnp* transistor operates in a manner similar to that of the *npn* device. The current in the *pnp* transistor is mainly conducted by holes. The current-voltage relationship will be identical to those of *npn* transistor except that v_{BE} has to be replaced by v_{EB}. The models for the *pnp* transistors are represented in the next figure; the *pnp* transistors controlled trough base is drawn with the emitter on top so that the currents to flow from top to bottom.



Different Modes of operation of the BJT

To illustrate the different modes of operation of BJT, we consider the simple circuit in the next figure. For different input voltages domains the transistor can operate in: cutoff, active and saturation regime.



VKL on input and output loops are valid for all modes of operation of the BJT: $v_I = R_B \cdot i_B + v_{BE}$ $V_{CC} = R_C \cdot i_C + v_O$.

Cuttoff Regime

Theoretically, the transistor is cuttoff if its junctions are reverse bias: $v_{BE}<0$ and $v_{CB}>0$.
The experimental cuttoff conditions are $v_{BE}<V_{D0}$ and $v_{CE}>V_{CEsat}$; where $V_{D0}=0.5\ldots0.6\ \text{V}$ is the threshold voltage of the EBJ (above which the current is insignificant – in the μA range) and $V_{CEsat}=0.2\ldots0.4\ \text{V}$ is the C-E saturation voltage.
For the transistor in cutoff region, all the BJT curents are very small and will be considered to be zero: $i_B=0$; $i_C=0$ and $i_E=0$.
From the VKL with the previos currents, the input and output voltages are:
$v_I = R_B \cdot i_B + v_{BE} = v_{BE} < V_{D0}$ and $v_O = V_{CC} - R_C \cdot i_C = V_{CC}$.
To conclude, for $v_I<V_{D0}$, $v_O=V_{CC}$.

Active Regime

Theoretically, the transistor is in active mode for: $v_{BE}>0$ and $v_{CB}>0$.
The experimental active regime conditions are $v_{BE}>V_D$ and $v_{CE}>V_{CEsat}$; with $V_D=0.6\ldots0.7\ \text{V}$ the voltage drop over the EBJ and $V_{CEsat}=0.2\ldots0.4\ \text{V}$ is the C-E saturation voltage.

For $v_I>V_D$ we get $i_B = \dfrac{v_I - V_D}{R_B}$. For the BJT in active mode, $i_C = \beta \cdot i_B$ and

$$v_O = V_{CC} - R_C \cdot i_C = V_{CC} - R_C \beta \frac{v_I - V_D}{R_B} = V_{CC} - \frac{\beta \cdot R_C}{R_B}(v_I - V_D).$$

That relationship indicates a linear function between output and input voltage.
Finally, verify the second condition: $v_{CE}>V_{CEsat}$ with $v_{CE}=v_O$, $v_O>V_{CEsat}$. If this relationship is not satisfied, the transistor is in saturation regime.

Saturation regime

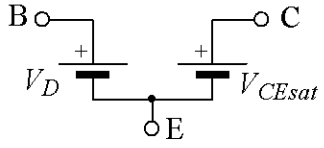
In saturation mode the collector current reaches its maximum value:

$$I_{Csat} = \frac{V_{CC} - V_{Csat}}{R_C} \cong \frac{V_{CC}}{R_C} = I_{C\max}.$$

At the border between active mode and saturation mode, the current in the base that is necessary to sustain the corresponding collector current is:

$$I_{Bsat} = \frac{I_{Csat}}{\beta} \cong \frac{I_{C\max}}{\beta}.$$

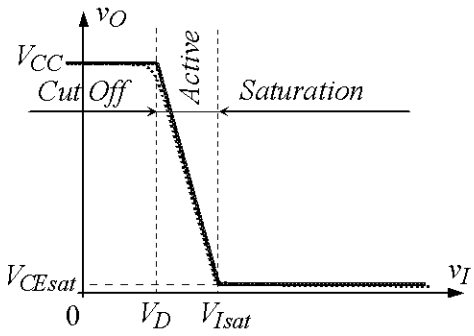
The actual current in the base depends on the base circuit: $i_B = \dfrac{v_I - V_D}{R_B}$, and its value can be increase above I_{Bsat}. The additional base current: $\Delta i_B = i_B - I_{Bsat}$ will open the CBJ; this junction become forward bias with $V_{BC}=0.4\ldots0.5\ \text{V}$. As a result the C-E voltage reaches its saturation value: $v_{CE}=v_{CB}+v_{BE}=\ v_{CB}-v_{BC}=0.7-0.4\ldots0.5\ \text{V}=0.2\ldots0.4\ \text{V}=V_{CEsat}$. For quick approximate calculations one may consider $V_{CEsat}=0$.
The model for *npn* saturated BJT is indicated in the next figure.



Transistor Inverter

The voltage transfer characteristic (VTC) of the circuit used to analyze different modes of operation of the BJT has three regions: cutoff, linear and saturation. In the next figure an

idealised VTC is indicated by the continues line (dark blue) and a real VTC is indicated by the dotted line. For switching applications the transistor is usually operated in cutoff and saturation (the C-E switch in the off and in the on state respectively). In both cutoff and saturation the transistor currents and voltages are well definedand do not depend on β. The power dissipated in the transistor: $P_d = v_{CE} \cdot i_C$ in these modes of operation is minimal; in cutoff the current is zero and in saturation the voltage is almoust zero.



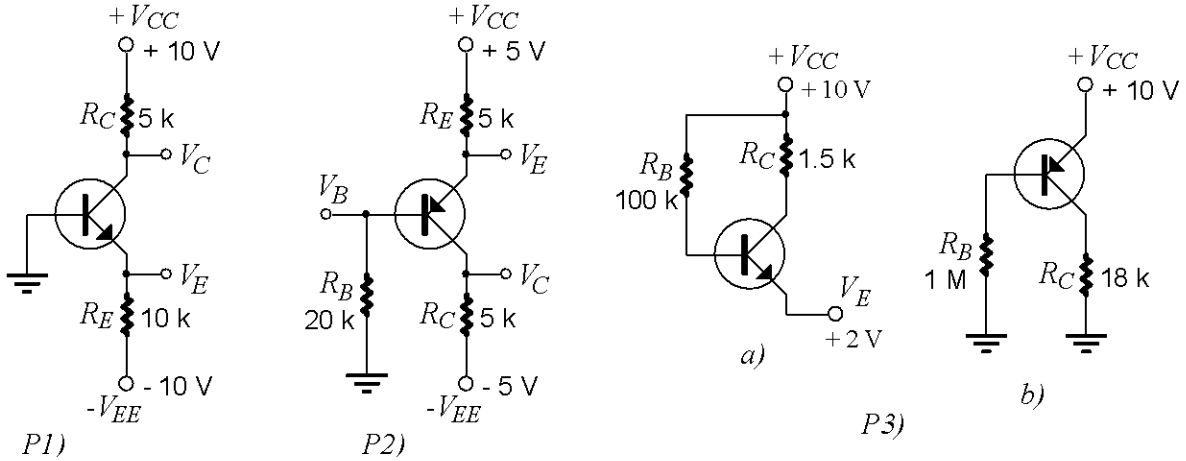
The circuit is the basic transistor logic inverter: if the input is low (voltage) the output is high (voltage) and if the input is high (voltage) the output is low (voltage).
For analog applications (such is amplification) the transistor is operated in active regim. Amplification is the process of linearly increasing the amplitude of an electrical signal. The transistor must be dc biased in order to operate as an amplifier. Improper biasing leads to distortion of the output.

The Superposition Theorem for ac-dc Circuits

In a transistor amplifier, the *dc* sources set up the *dc* currents and voltages. The *ac* sources produce fluctuations in the transistor currents and voltages. The simplest way to analyse transistor circuits is to split the analyse into two parts: a *dc* analysis and an *ac* analysis – applying the superposition theorem in a special way. We take all *dc* sources at the same time and work out the *dc* currents and voltages. Next, take all *ac* sources at the same time and calculate the *ac* currenats and voltages. Here are the steps:

1. Reduce all *ac* sources to zero and open all capacitors. The circuit that remains is the dc equivalent circuit. Using this circuit we calculate whatever *dc* currents and voltages we are interest in.
2. Reduce all *dc* sources to zero and short all coupling and bypass capacitors. The circuit that remains is the *ac* equivalent circuit (and this is all that matters as far as *ac* currents and voltagea are concerned). This is the circuit to use to compute in calculating *ac* currents and voltages.
3. By adding the *dc* and *ac* currents and voltages we get the total currents and voltages. Ussualy, this 3rd phase is not really necessary as long *as* only ac (signal) voltiges (or current) is what we need.

Applications



S5 – P1. In the circuit shown in figure (*P1*) the voltage at the emitter was measured: $v_E = -0.7\,\text{V}$. If $\beta = 50$, find I_E, I_B, I_C, V_C and α.

$$I_E = \frac{V_E - (-V_{EE})}{R_E} = \frac{-0.7+10}{10k} = 0.93\,\text{mA}.\quad I_B = \frac{I_E}{\beta+1} = \frac{0.93}{51} = 18.2\,\mu\text{A}.\quad I_C = I_E - I_B = 0.912\,\text{mA}.$$

$$V_C = V_{CC} = R_C I_C = 10 - 0.912m \cdot 5k = 5.44\,\text{V}.\ (V_{CE} > V_{CEsat}),\ \alpha = \frac{I_C}{I_E} = \frac{\beta}{\beta+1} = 0.98\,.$$

S5 – P2. A single measurement indicates the emitter voltage in the circuit of figure (*P2*) to be $1.0\,\text{V}$. Under the assumption that $v_{EB} = V_D = 0.7\,\text{V}$ what are: I_B, I_C, I_E, V_C, β and α. (Isn't it surprising what only one measurement can do?)

$$I_B = \frac{V_B}{R_C} = \frac{V_E - V_{BE}}{R_B} = \frac{1-0.7}{20k} = 0.015\,\text{mA} = 15\,\mu\text{A},\ I_E = \frac{V_{CC} - V_E}{R_E} = \frac{5-1}{5k} = 0.8\,\text{mA}.$$

$$I_C = I_E - I_B = 0.785\,\text{mA},\ V_C = -V_{EE} + R_C I_C = -5 + 5k \cdot 0.785m = -1.075\,\text{V},$$

$$V_{CE} = V_C - V_E = 2.075\,\text{V}\ (> V_{CEsat}),\ \beta = \frac{I_C}{I_B} = \frac{785\mu}{15\mu} = 52.3\,,\ \alpha = \frac{I_C}{I_E} = \frac{785\mu}{800\mu} = 0.98\,.$$

S5 – P3. Identify wheather the circuits in figures (*P3*) operate in the active or saturation mode. What is the base voltage in each case? If active, what is the collector voltage? Consider $V_D = 0.7\,\text{V}$ and the cases with $\beta = 50$ and $\beta = 100$.

$$a)\ V_B = V_E + V_{BE} = V_E + V_D = 2.7\,\text{V},\ I_B = \frac{V_{CC} - V_B}{R_B} = \frac{12-2.7}{100k} = 93\,\mu\text{A}.$$

$$I_{C\max} = \frac{V_{CC} - V_E}{R_C} = \frac{12-2}{1.5k} = 6.7\,\text{mA},\ I_{Bsat} = \frac{I_{C\max}}{\beta} = \frac{6.7}{50...100} = 134\,\mu\ldots 67\,\mu\text{A},$$

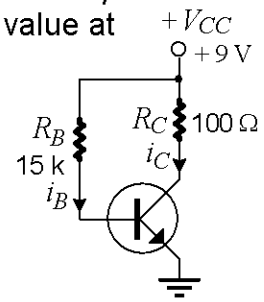
- For $\beta = 50$, $I_B < I_{Bsat}$ ($93\,\mu < 134\,\mu\text{A}$), the BJT is in the active mode and $V_C = V_{CC} - R_C I_C = V_{CC} - R_C \beta \cdot I_B = 12 - 1.5k \cdot 50 \cdot 93\mu = 5.025\,\text{V}.$
- For $\beta = 100$, $I_B > I_{Bsat}$ ($93\,\mu > 67\,\mu\text{A}$), the BJT is in the saturation mode.

b) $V_B = V_E - V_{EB} = V_{CC} - V_D = 10 - 0.7 = 9.3\,\text{V},\ I_B = \dfrac{V_B}{R_B} = \dfrac{9.3}{1M} = 9.3\,\mu\text{A}.$

$I_{C\max} = \dfrac{V_{CC}}{R_C} = \dfrac{10}{18k} = 0.56\,\text{mA},\ I_{Bsat} = \dfrac{I_{C\max}}{\beta} = \dfrac{0.56}{50...100} = 11\mu...5.6\mu\text{A},$

- For $\beta = 50$, $I_B < I_{Bsat}$ (9.3 μ<11 μA), the BJT is in the active mode and $V_C = R_C I_C = R_C \beta \cdot I_B = 18k \cdot 50 \cdot 9.3\mu = 8.37\,\text{V}.$
- For $\beta = 100$, $I_B > I_{Bsat}$ (9.3 μ>5.6 μA), the BJT is in the saturation mode.

S5 – P4. The data sheet for a particular transistor specifies a minimum β of 50 and a maximum β of 130, $v_{BE} = V_D = 0.7$ V and $V_{CEsat} = 0.3$ V.
a) What range of Q point can be expected if an attempt is made to mass-produce the circuit in figure. Is this range acceptable?
b) The base bias circuit is subject to a temperature variation from 0 to 70°C. The β decreases by 20% at 0°C and increases by 35% at 70°C from its nominal value at 25°C. Compute the Q point limits for the specified temperature range.



a) $I_B = \dfrac{V_{CC} - v_{BE}}{R_B} = \dfrac{V_{CC} - V_D}{R_B} = \dfrac{9 - 0.7}{15k} = 0.553\,\text{mA}.$

$I_C = \beta \cdot I_B = (50...130) \cdot 0.553m = 28...72\ \text{mA}.$

$V_{CE} = V_{CC} - R_C I_C = 9 - 0.1k \cdot (28...72)m = 6.2...1.8\,\text{V}.$

This range of Q point is not acceptable because of the big variations of I_C and V_{CE}.

b) $\beta_{\min} = 0.8 \cdot 50 = 40$, $\beta_{\max} = 1.35 \cdot 130 = 175.5$;

$I_{C\min} = \beta_{\min} \cdot I_B = 40 \cdot 0.553m = 22\,\text{mA}$, $V_{CE\max} = V_{CC} - R_C I_{C\max} = 9 - 0.1k \cdot 22m = 6.8\,\text{V}.$

$I_{C\max} = \beta_{\max} \cdot I_B = 175.5 \cdot 0.553m = 97\,\text{mA}$, $V_{CE\min} = V_{CC} - R_C I_{C\max} = 9 - 0.1k \cdot 97m = -0.7\,\text{V}.$

A negative value for V_{CE} is not possible; it means that the transistor is saturated. The maximum I_C and maximum β in active mode are:

$I_{C\max} = \dfrac{V_{CC} - V_{CEsat}}{R_C} = \dfrac{9 - 0.3}{0.1k} = 87\,\text{mA}$, $\beta = \dfrac{I_{C\max}}{I_B} = \dfrac{87m}{0.553m} = 157$. For $\beta > 157$ the circuit will saturate the BJT and the corresponding Q point is: $I_C = 87$ mA and $V_{CE} = V_{CEsat} = 0.3$ V.